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BASIC OF ELECTRONICS

Lecture 10

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Applied Informatics

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R_{Sac} is the only unknown in this equation. Therefore,

$$R_{Sac} = -\frac{R_L \| R_D}{A_v} - \frac{1}{g_m}$$

Suppose now that R_{Sac} is found to be positive but less than R_{Sdc}. This is the desirable condition since

$$R_{Sdc} = R_{Sac} + R_{S2}$$

Then our design is complete and

$$R_1 = R_{\text{in}} = R_G$$

Step 10 Suppose that R_{Sac} is found to be positive but *greater* than R_{Sdc}. The amplifier cannot be designed with the voltage gain and Q-point as selected. A new Q-point must be selected, and we return to Step 1. If the voltage gain is too high, it may not be possible to effect the design with any Q-point. A different transistor may be needed or the use of two separate stages may be required.

4.8 Selection of Components

A design is not yet complete when the various component values are specified. It is still necessary to select the actual components to be used (e.g., choose the manufacturer's part numbers from a catalog). Thus, when the design requires a resistor value, say 102.5 Ω, the designer will not be able to find this resistor in a standard parts catalog. Available nominal component values depend upon tolerances. As an example, a 100-Ω resistor with a 5% tolerance can have any value between 95 Ω and 105 Ω. It would not make much sense for the manufacturer to offer another off-the-shelf resistor with a nominal rating of 101 Ω, since that resistor could have a value between approximately 96 Ω and 106 Ω. The distance between adjacent nominal component values is therefore related to the tolerance, with such distance decreasing as the tolerance decreases (i.e., higher-precision components). Standard values of resistors and capacitors are included in Appendix E.

Since component values are not readily available to any degree of resolution, it would not make sense to carry out design calculations to an unreasonably large number of significant figures.

In our design examples, we specify values to at least three significant figures. This is important to ensure that we still maintain accuracy to two significant

figures following arithmetic operations. For example, suppose we must add

$$0.274 + 0.474$$

If these two numbers are rounded to two significant figures, we obtain

$$0.27 + 0.47 = 0.74$$

If we first do the calculation, however, we obtain

$$0.274 + 0.474 = 0.748$$

which rounds to 0.75. Rounding the numbers prior to performing the addition results in an error in the second significant figure. Thus, to reduce accumulated errors and to increase the confidence that our answers are accurate to two significant figures, we maintain at least three figures throughout the calculations.

Example 4.5 JFET CS Amplifier (Design)

Design a CS JFET amplifier with a voltage gain of $A_v = -4$, $R_{in} = 100$ kΩ, $R_L = 20$ kΩ, $I_{DSS} = 6.67$ mA, $V_p = -3.33$ V and $V_{DD} = 20$ V. Since we do not know whether we will need an R_2, let us start with Figure 4.15(a) and the dimensionless curves of Figure 4.8.

SOLUTION

Step 1 The Q-point is selected from Figure 4.8 as follows:

$$I_{DQ} = \frac{I_{DSS}}{2} = 3.33 \text{ mA}$$

$$V_{GSQ} = 0.3V_p = -1 \text{ V}$$

$$V_{DSQ} = \frac{V_{DD}}{2} = 10 \text{ V}$$

Then

$$g_m = 1.42 \frac{I_{DSS}}{V_p} = 2.86 \times 10^{-3} \text{ S}$$

and

$$\frac{1}{g_m} = 350\ \Omega$$

Step 2 From Step 2 in the design procedure, we have

$$R_D + R_{Sdc} = \frac{20\ \text{V} - 10\ \text{V}}{3.33\ \text{mA}} = 3\ \text{k}\Omega = K_1$$

Step 3 Using the ac gain equation, we obtain

$$A_v = \frac{-(20\ \text{k}\Omega \parallel R_D)}{(3\ \text{k}\Omega - R_D) + 350\ \Omega} = -4$$

$$R_D^2 + (21.65\ \text{k}\Omega)R_D - 67\ \text{M}\Omega^2 = 0$$

From the quadratic for R_D we select the positive root,

$$R_D = 2.747\ \text{k}\Omega$$

Step 4 This quantity is less than K_1, so we proceed to Step 4. We find R_S using equation (4.15):

$$R_S = 3\ \text{k}\Omega - R_D = 253\ \Omega$$

Step 5 This step now yields

$$V_{GG} = -1 + 253(3.33 \times 10^{-3}) = -0.15\ \text{V}$$

Since this negative voltage cannot be obtained by dividing the source voltage using resistors, we skip to Step 7.

Step 7 Let

$$R_2 \rightarrow \infty$$

Then

$$V_{GG} = 0 = V_{GSQ} + I_{DQ}R_{Sdc}$$
$$= -1 + (3.33 \times 10^{-3})R_{Sdc}$$

Solving for R_{Sdc} we obtain

$$R_{Sdc} = 300\ \Omega$$

Step 8 This step yields

$$R_D = 3\ \text{k}\Omega - R_{Sdc} = 2.7\ \text{k}\Omega$$

R_{Sac} is determined from Step 9.

Step 9

$$R_{Sac} = -\frac{R_L \parallel R_D}{A_v} - \frac{1}{g_m} = \frac{-(20\ \text{k}\Omega \parallel 2.7\ \text{k}\Omega)}{-4} - 350\ \Omega = 245\ \Omega$$

The final circuit is shown in Figure 4.16, where the component values are

$$R_D = 2.7\ \text{k}\Omega$$

$$R_{S1} = R_{Sac} = 245\ \Omega$$

$$R_{S2} = R_{Sdc} - R_{Sac} = 300\ \Omega - 245\ \Omega = 55\ \Omega$$

$$R_G = R_{\text{in}} = R_1 = 100\ \text{k}\Omega$$

Example 4.6 JFET CS Amplifier (Design)

Repeat Example 4.5 for Figure 4.17, but select a Q-point that is not in the center of the linear region.

SOLUTION Let us arbitrarily select the new operating point as follows.

Step 1

$$I_{DQ} = 3.5\ \text{mA}$$

$$V_{GSQ} = -0.8\ \text{V}$$

$$V_{DSQ} = 6\ \text{V}$$

Then

$$g_m = 2.0 \times 10^{-3}\ \text{S}$$

and

$$\frac{1}{g_m} = 500\ \Omega$$

Step 2 This step in the design procedure yields

$$R_D + R_S = \frac{20 - 6}{3.5 \times 10^{-3}} = 4\ \text{k}\Omega = K_1$$

Step 3 Then we find

$$A_v = -4 = \frac{-R_D \parallel 20\ \text{k}\Omega}{4\ \text{k}\Omega - R_D + 500\ \Omega}$$

from which we obtain, after solving the quadratic equation,

$$R_D = 3.716\ \text{k}\Omega$$

This quantity is less than K_1, so we proceed to Step 4.

Step 4 From equation (4.17), we obtain

$$R_S = 4\ \text{k}\Omega - 3.716\ \text{k}\Omega = 284\ \Omega$$

Step 5 Using the bias equation of this step, we find

$$V_{GG} = -0.8 + 284(3.5 \times 10^{-3}) = 0.194\ \text{V}$$

Step 6 To determine R_1 and R_2 with $R_{\text{in}} = R_G$, we use Step 6, since V_{GG} is the same polarity as V_{DD}. (This contrasts with the situation in the previous example.) Thus,

$$R_1 = \frac{100\ \text{k}\Omega}{1 - 0.194/20} = 101\ \text{k}\Omega$$

$$R_2 = 100\ \text{k}\Omega \left(\frac{20}{0.194}\right) = 10.3\ \text{M}\Omega$$

The final circuit is shown in Figure 4.17.

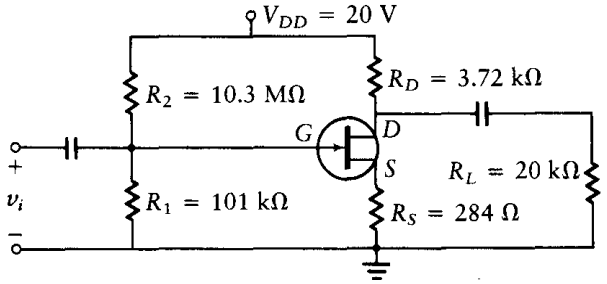


Figure 4.17
CS amplifier for Example 4.6.

Example 4.7 JFET CS Amplifier (Analysis)

Analyze the single-stage JFET CS amplifier shown in Figure 4.18 and determine A_v, A_i, and R_{in}. Assume $I_{DSS} = 2$ mA and $V_p = -2$ V.

SOLUTION We first calculate the Q-point, from which we determine g_m; both A_v and A_i depend upon this parameter. Remember that the value of g_m depends upon the Q-point location. We need two equations in order to find I_{DQ} and V_{GSQ}, as follows:

$$V_{GSQ} = -R_S I_{DQ} = -0.4 I_{DQ}$$

and from equation (4.1),

$$\frac{I_{DQ}}{I_{DSS}} = \left(1 - \frac{V_{GSQ}}{V_p}\right)^2$$

When we solve these two equations, we obtain a quadratic equation in I_{DQ}.

$$\frac{I_{DQ}}{2} = \left(1 - \frac{-0.4 I_{DQ}}{-2}\right)^2$$

where I_{DQ} is in milliamps.

This reduces to

$$I_{DQ}^2 - 22.5 I_{DQ} + 25 = 0$$

We solve this quadratic equation and obtain two values: 21.33 mA and 1.17 mA. Since I_{DSS} is only 2 mA, we discard the larger value and obtain

$$I_{DQ} = 1.17 \text{ mA}$$

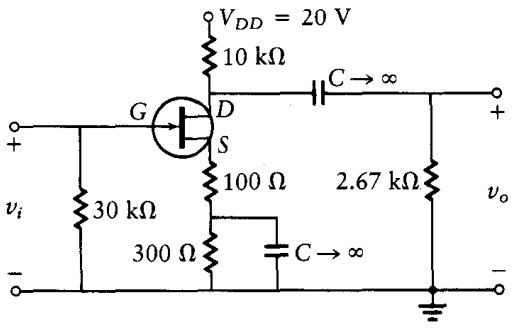


Figure 4.18
CS amplifier for Example 4.7.

Hence

$$V_{GSQ} = (-0.4)(I_{DQ}) = -(0.4)(1.17) = -0.469 \text{ V}$$

We use equation (4.3) to find g_m as follows:

$$g_m = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GSQ}}{V_p}\right) = \frac{(2)(2)}{-(-2)}\left(1 - \frac{-0.469}{-2}\right) = 1.53 \text{ mS}$$

and

$$\frac{1}{g_m} = 653\ \Omega$$

We now find the voltage gain from equation (4.16a):

$$A_v = -\frac{R_D \parallel R_L}{R_{Sac} + 1/g_m} = \frac{10\ \text{k}\Omega \parallel 2.67\ \text{k}\Omega}{100\ \Omega + 653\ \Omega} = -2.8$$

and

$$R_{\text{in}} = 30\ \text{k}\Omega$$

$$A_i = \frac{A_v R_{\text{in}}}{R_L} = \frac{-2.8(30{,}000)}{2670} = -31.5$$

Drill Problems

D4.1 Design a CS JFET amplifier that has an R_L of 10 kΩ, $V_{DD} = 12$ V, $R_{\text{in}} = 500$ kΩ, and $A_v = -2$. Use the circuit of Figure 4.15(a). Select the Q-point as $V_{DSQ} = 6$ V, $V_{GSQ} = -1$ V, $I_{DQ} = 1$ mA, and $g_m = 2500$ μS.

Ans: $R_S = 1.22$ kΩ; $R_D = 4.78$ kΩ;
$R_1 = 509$ kΩ; $R_2 = 27$ MΩ;
$A_i = -100$

D4.2 Redesign the amplifier of Problem D4.1 for a Q-point at $V_{DSQ} = 7$ V, $V_{GSQ} = -1.2$ V, $I_{DQ} = 0.5$ mA and $g_m = 3330$ μS.

Ans: $R_1 = 500$ kΩ; $R_2 = \infty$;
$R_D = 7.6$ kΩ; $R_{Sdc} = 2.4$ kΩ;
$R_{Sac} = 1.86$ kΩ; $A_i = -100$

4.9 Analysis of CD (SF) Amplifiers

The CD (SF) JFET amplifier is illustrated in Figure 4.19(a) and the equivalent circuit is shown in Figure 4.19(b). Our approach to the analysis of this amplifier parallels that of Section 4.7. The input resistance is $R_{\text{in}} \approx R_G$. Note in the equivalent circuit that we ignore r_{DS}, since it is usually much larger than R_S. If r_{DS} is not much larger than R_S, we modify the following equations by replacing R_S with $r_{DS} \parallel R_S$.

Writing KVL equation around the gate-to-source loop, we have

$$v_{gs} = v_i - g_m(R_S \parallel R_L)v_{gs}$$

from which we obtain

$$v_i = v_{gs}\,[1 + g_m(R_S \parallel R_L)]$$

The output voltage is

$$v_o = g_m(R_S \parallel R_L)v_{gs}$$

and the voltage gain is the ratio

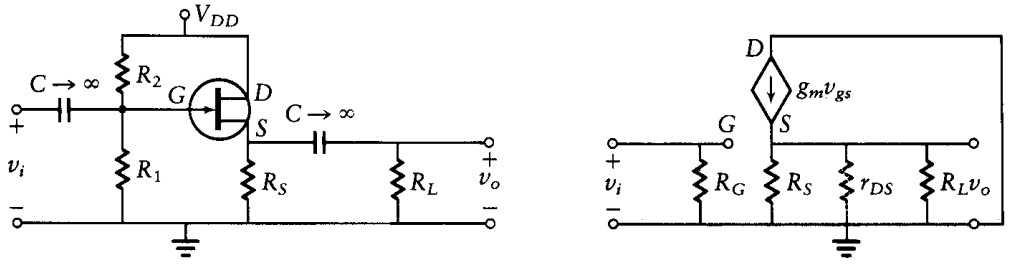
$$A_v = \frac{v_o}{v_i} = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)} = \frac{R_S \parallel R_L}{(R_S \parallel R_L) + 1/g_m} \tag{4.19a}$$

Note that since $R_S \parallel R_L$ is of the same magnitude as $1/g_m$, the voltage gain of a SF amplifier is less than unity.

We find the current gain using the gain impedance formula as follows:

$$\begin{aligned} A_i &= A_v \frac{R_{\text{in}}}{R_L} \\ &= \frac{R_S \parallel R_L}{(R_S \parallel R_L) + 1/g_m} \frac{R_{\text{in}}}{R_L} = \frac{R_S}{(R_S \parallel R_L) + 1/g_m} \frac{R_G}{R_S + R_L} \end{aligned} \tag{4.19b}$$

Figure 4.19 JFET SF amplifier.



(a) Amplifier (b) Equivalent circuit

4.10 CD Amplifier Design Procedure

In this section, we present the design procedure for the CD JFET amplifier. This procedure is the same as that used to design depletion MOSFET amplifiers. The following quantities are specified: current gain, load resistance, and V_{DD}. Input resistance may be specified instead of current gain. With A_i (or R_{in}) specified, we have three equations (two loop equations and the A_i equation) in three unknowns, R_1, R_2 and R_S. In this case, we refer to Figure 4.19(a).

If both A_i and R_{in} are specified, then we have four equations and only three unknowns. With one more equation than the number of unknowns, it usually will not be possible to find a solution without modifying the circuit. In such cases, we introduce a bypass capacitor across a portion of R_S, as shown in Figure 4.20. With that change, we now have four unknowns, R_1, R_2, R_{S1}, and R_{S2}, so the circuit can be solved.

Step 1 Select a Q-point in the center of the FET characteristic curves with the aid of Figure 4.8. This step determines V_{DSQ}, V_{GSQ}, I_{DQ}, and g_m.

Step 2 Write the dc KVL equation around the drain-to-source loop.

$$V_{DD} = V_{DSQ} + R_S I_{DQ}$$

from which we find the dc value of R_S,

$$R_{Sdc} = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} \tag{4.20a}$$

Step 3 Find R_{Sac} from the rearranged current gain equation, equation (4.19b), as follows:

$$R_{Sac} = \frac{R_L}{(R_G/A_i - R_L)g_m - 1} \tag{4.20b}$$

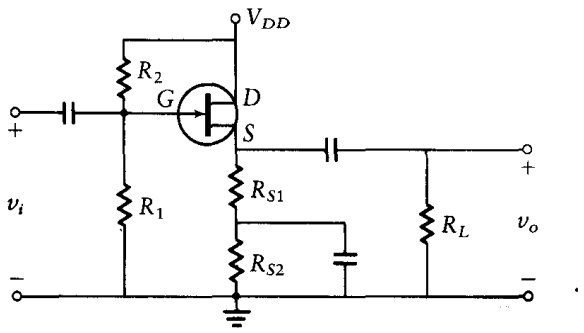


Figure 4.20
CD amplifier.

where

$$R_G = R_{in}$$

If the input resistance is not specified, let $R_{Sac} = R_{Sdc} = R_S$ and calculate the input resistance from equation (4.20b). If the input resistance is not high enough, it may be necessary to change the Q-point location.

If R_{in} is specified, it is necessary to calculate R_{Sdc} from equation (4.20a) and R_{Sac} from equation (4.20b). In such cases, R_{Sac} is different from R_{Sdc}, so we bypass part of R_S with a capacitor.

Step 4 Determine V_{GG} using the equation

$$V_{GG} = V_{GSQ} + I_{DQ}R_S$$

No phase inversion is produced in a source-follower FET amplifier, and V_{GG} is normally the same polarity as the supply voltage.

Step 5 Determine the values of R_1 and R_2 from equation (4.12):

$$R_1 = \frac{R_G}{1 - V_{GG}/V_{DD}}$$

$$R_2 = \frac{R_G V_{DD}}{V_{GG}}$$

There is usually enough drain current in an SF to develop the opposite polarity voltage needed to offset the negative voltages required by the JFET gate. Therefore, normal voltage division biasing can be used.

We now return to the problem of specifying the input resistance. We can assume that part of R_S is bypassed, as in Figure 4.20, which leads to different values of R_{Sac} and R_{Sdc}. Step 2 is used to solve for R_{Sdc}. In Step 3, we let R_G equal the specified value of R_{in} and use equation (4.20b) to solve for R_{Sac}.

If the R_{Sac} calculated above is smaller than R_{Sdc}, the design is accomplished by bypassing R_{S2} with a capacitor. Remember that $R_{Sac} = R_{S2}$ and $R_{Sdc} = R_{S1} + R_{S2}$. If, on the other hand, R_{Sac} is larger than R_{Sdc}, the Q-point must be moved to a different location. We select a smaller V_{DSQ}, thus causing increased voltage to be dropped across $R_{S1} + R_{S2}$, which makes R_{Sdc} larger. If V_{DSQ} cannot be reduced sufficiently to make R_{Sdc} larger than R_{Sac}, then the amplifier cannot be designed with the given current gain, R_{in}, and FET type. One of these three specifications must be changed, or a second amplifier stage must be used to provide the required gain.

Example 4.8 CD Amplifier (Design)

Design a CD JFET amplifier with the following specifications: $A_i = 12$, $R_L = 400\ \Omega$, $I_{DSS} = 20$ mA, $V_p = -6.67$ V, and $V_{DD} = 12$ V.

SOLUTION

Step 1 Select the Q-point as follows (see Figure 4.8):

$$I_{DQ} = \frac{I_{DSS}}{2} = 10 \text{ mA}$$

$$V_{DSQ} = \frac{V_{DD}}{2} = 6 \text{ V}$$

$$V_{GSQ} = (0.3)(-6.67) = -2 \text{ V}$$

$$g_m = \frac{1.42 I_{DSS}}{V_p} = 4.26 \text{ mS}$$

and

$$\frac{1}{g_m} = 235\ \Omega$$

Step 2 Since no value of R_{in} is specified, $R_S = R_{Sac} = R_{Sdc}$ and we use Figure 4.19, with the result

$$R_S = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} = \frac{12 - 6}{10 \times 10^{-3}} = 600\ \Omega$$

Step 3 We use this step to find R_G by rearranging equation (4.19b):

$$R_G = A_i \left[R_L + \frac{1 + R_L/R_S}{g_m} \right] = 12 \left[400 + \frac{1 + 400/600}{4.26 \text{ mS}} \right] = 9.5 \text{ k}\Omega$$

Since R_G is greater than the minimum specified R_{in}, the design is acceptable and we can continue to Step 4.

Step 4

$$V_{GG} = -2 + (10 \times 10^{-3})(600) = 4 \text{ V}$$

Step 5 Finally, from this step we find

$$R_1 = \frac{9500}{1 - 4/12} = 14.25\ \text{k}\Omega$$

$$R_2 = \frac{9500 \times 12}{4} = 28.5\ \text{k}\Omega$$

$$A_v = A_i \frac{R_L}{R_{in}} = 12\,\frac{400}{9500} = 0.51$$

Example 4.9 CD Amplifier (Design)

Design a CD amplifier (see Figure 4.19) to meet the following specifications: $A_i = 20$, $R_{\text{in}} = 50\ \text{k}\Omega$, $R_L = 1\ \text{k}\Omega$, $V_{DD} = 12$ V, $I_{DSS} = 20$ mA, and $V_p = -6.67$ V. Determine all component values for the circuit.

SOLUTION The Q-point is selected as

$$V_{DSQ} = \frac{V_{DD}}{2} = 6\ \text{V}$$

$$I_{DQ} = \frac{I_{DSS}}{2} = 10\ \text{mA}$$

$$V_{GSQ} = 0.3(V_p) = -2\ \text{V}$$

We find g_m from the dimensionless curve of Figure 4.8 as follows:

$$g_m = 1.42\,\frac{I_{DSS}}{|V_p|} = 4.26\ \text{mS}$$

and

$$\frac{1}{g_m} = 230\ \Omega$$

We use Step 2 to find R_{Sdc}. Note that since R_{in} is given, we will probably need values for R_{Sdc} and R_{Sac}.

$$R_{Sdc} = \frac{12 - 6}{10 \times 10^{-3}} = 600\ \Omega$$

Since R_{in} is specified, we use Step 3 to find R_{Sac}; from equation (4.20),

$$R_G = R_{in} = 50\ \text{k}\Omega$$

$$R_{Sac} = \frac{R_L}{(R_G/A_i - R_L)g_m - 1}$$

$$= \frac{1000}{(50{,}000/20 - 1000)4.26\ \text{mS} - 1} = 186\ \Omega$$

Since R_{Sac} is less than R_{Sdc}, we find $R_{S1} = 186\ \Omega$ and $R_{S2} = 414\ \Omega$ in the configuration of Figure 4.20. We continue to Step 4.

$$V_{GG} = -2 + (10 \times 10^{-3})(600) = 4\ \text{V}$$

Finally, we use Step 5 to find R_1 and R_2:

$$R_1 = \frac{50{,}000}{1 - 4/12} = 75\ \text{k}\Omega$$

$$R_2 = \frac{50{,}000 \times 12}{4} = 150\ \text{k}\Omega$$

The design is complete.

Drill Problems

D4.3 Design a CD JFET amplifier as shown in Figure 4.19, with $R_L = 10$ kΩ, $R_{in} = 200$ kΩ, $V_{DD} = 12$ V and a Q-point selected to be at $V_{DSQ} = 6$ V, $V_{GSQ} = -1$ V, $I_{DQ} = 1$ mA, and $g_m = 4$ mS. Determine the value of resistors and the current gain of the amplifier.

Ans: $R_S = 6\ \text{k}\Omega$; $R_1 = 342\ \text{k}\Omega$;
$R_2 = 480\ \text{k}\Omega$; $A_i = 18.8$

D4.4 Design a CD JFET amplifier as shown in Figure 4.21 to provide a current gain of 15 to a load of $R_L = 20$ kΩ using $V_{DD} = 12$ V and $R_{in} = 400$ kΩ. Select a Q-point at $V_{DSQ} = 6$ V, $I_{DQ} = 2$ mA, $V_{GSQ} = -0.5$ V, and $g_m = 3330\ \mu\text{S}$.

Ans: $R_{Sdc} = 3\ \text{k}\Omega$; $R_{Sac} = 942\ \Omega$;
$R_1 = 873\ \text{k}\Omega$; $R_2 = 738\ \text{k}\Omega$