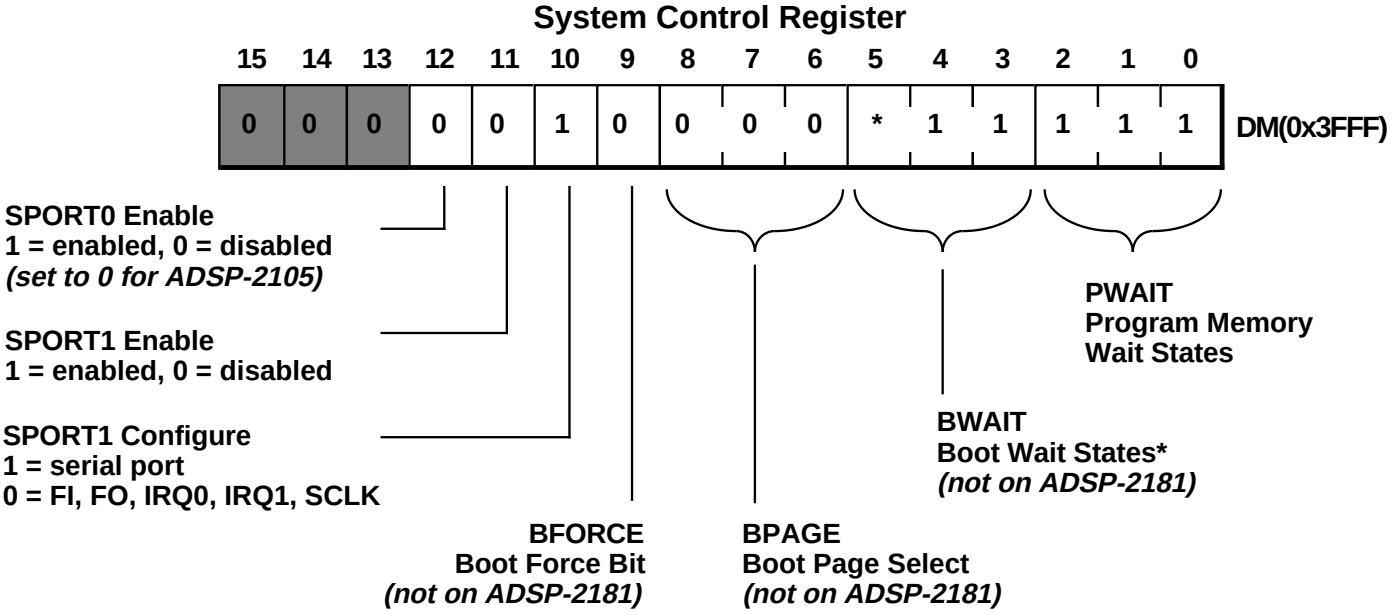
Control/Status Registers E

E.1 OVERVIEW

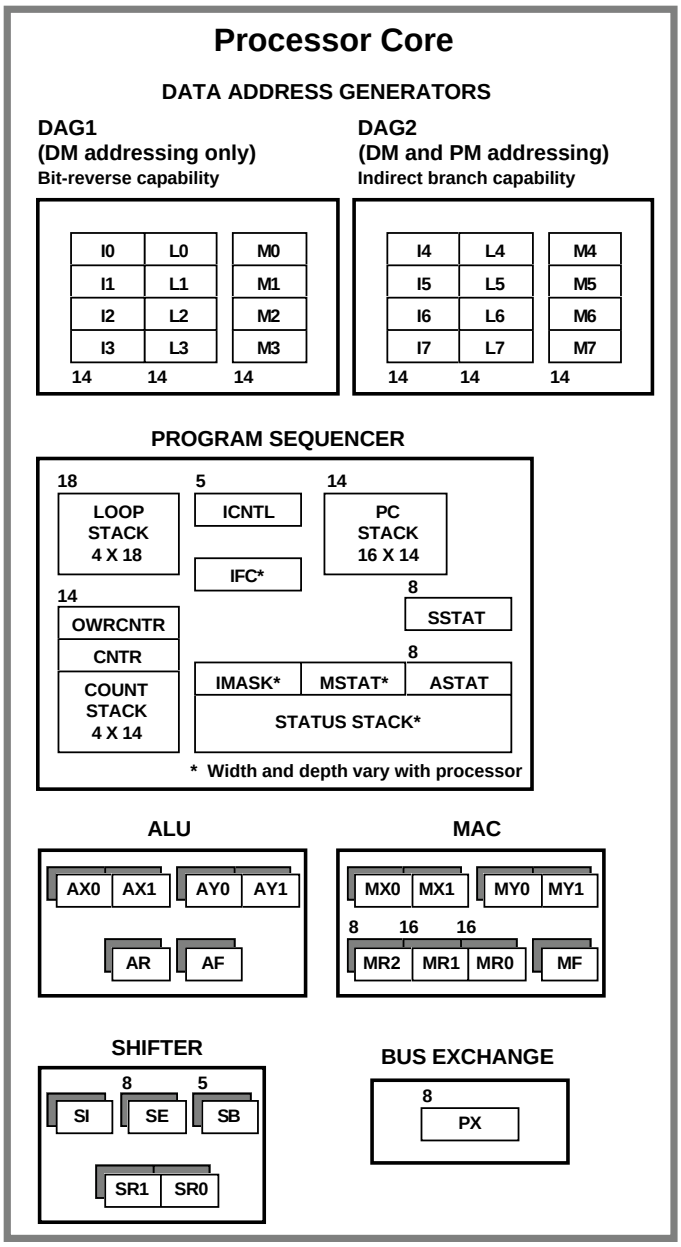
This appendix shows bit definitions for 1) the memory-mapped control registers and 2) other (non-memory-mapped) control and status registers of all ADSP-21xx processors. The memory-mapped registers are listed in descending address order. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a gray field. These bits should always be written with zeros.

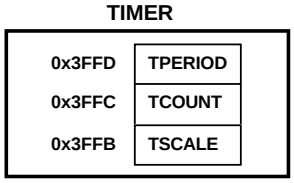
Memory-Mapped Registers

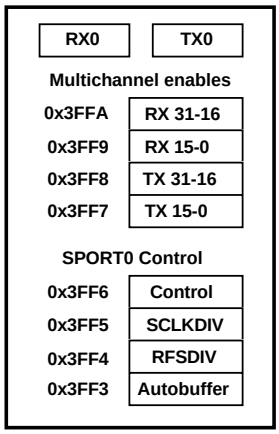


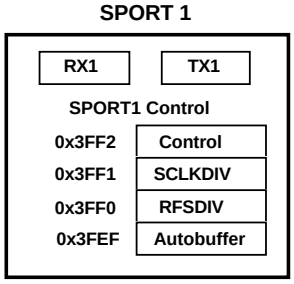
*** Bit 5 initialized to 1 on ADSP-2171, ADSP-21msp58/59**
Bit 5 initialized to 0 on ADSP-2101, ADSP-2105, ADSP-2115, ADSP-2111

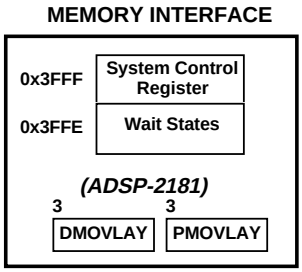
E Control/Status Registers

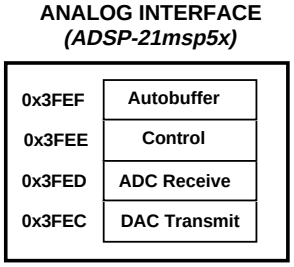


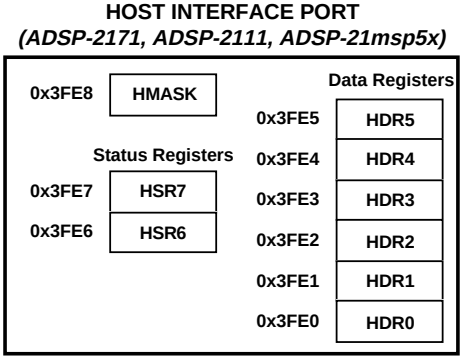


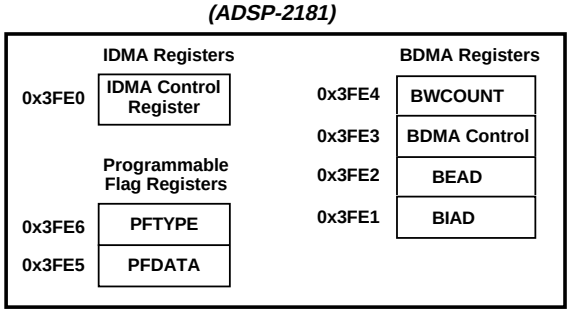








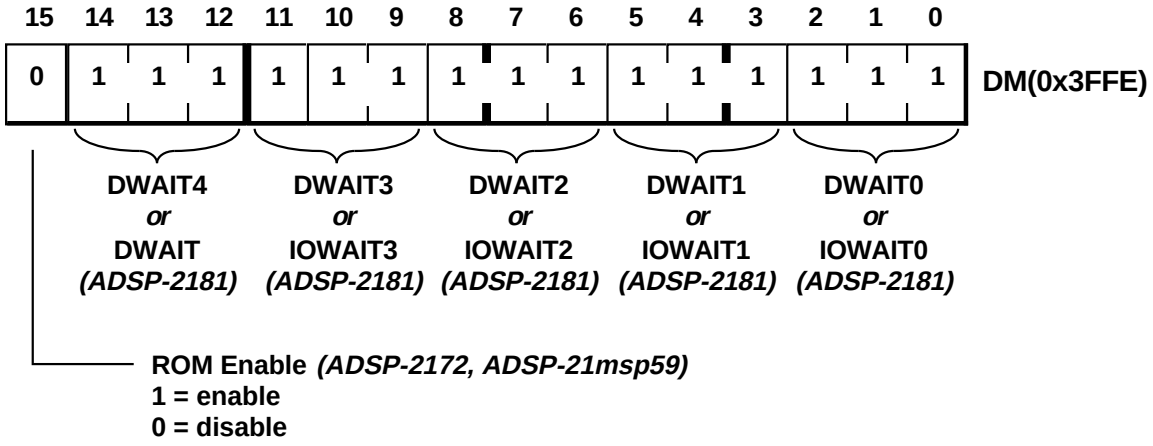




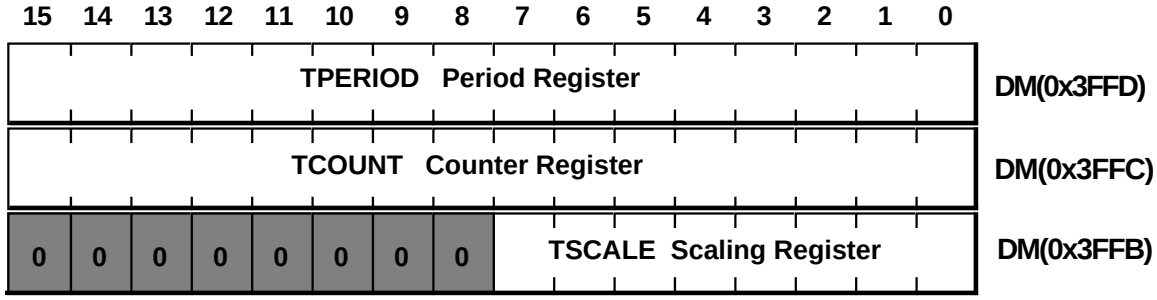
Control/Status Registers E

Memory-Mapped Registers

Waitstate Control Register



Timer Registers

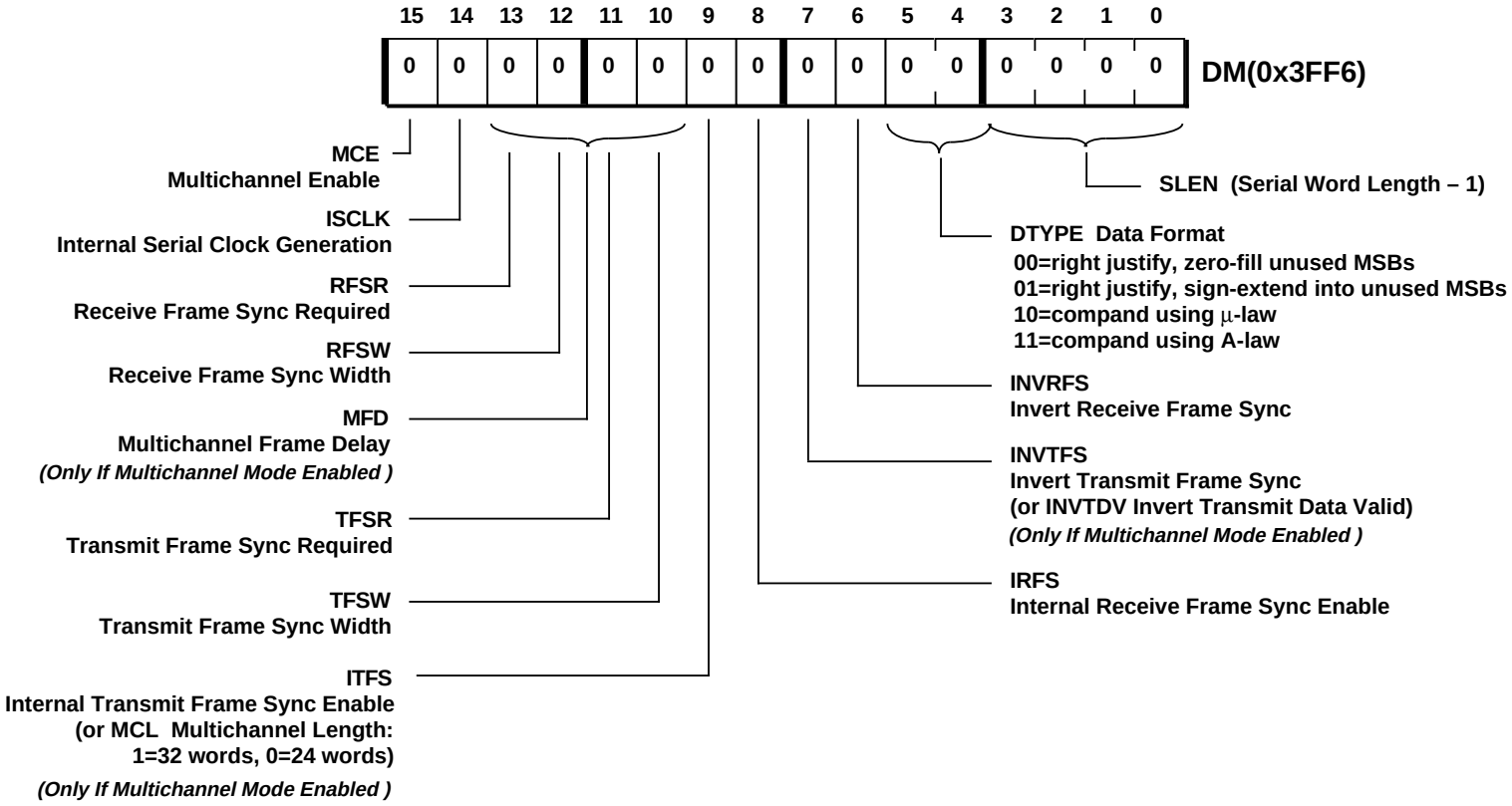


Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

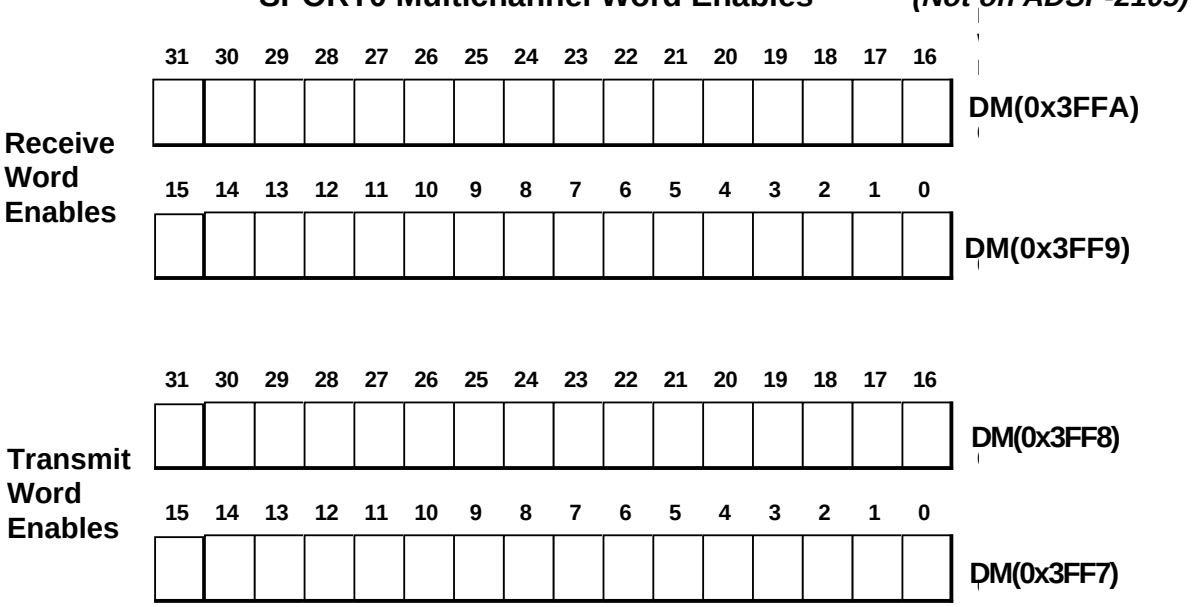
E Control/Status Registers

Memory-Mapped Registers

SPORT0 Control Register ***(Not on ADSP-2105)***



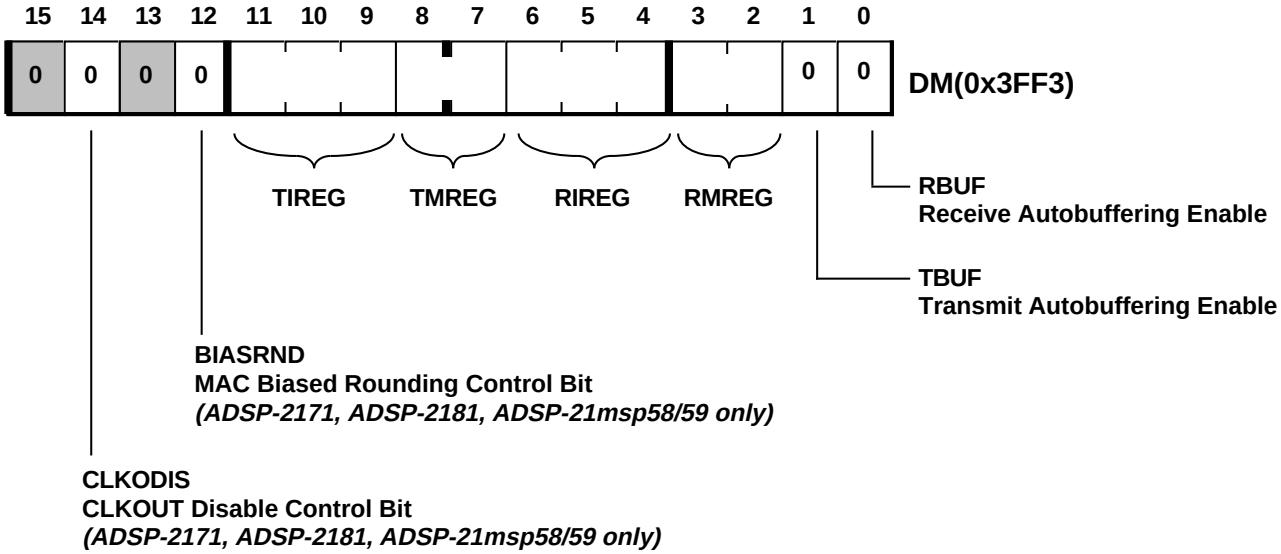
SPORT0 Multichannel Word Enables ***(Not on ADSP-2105)***



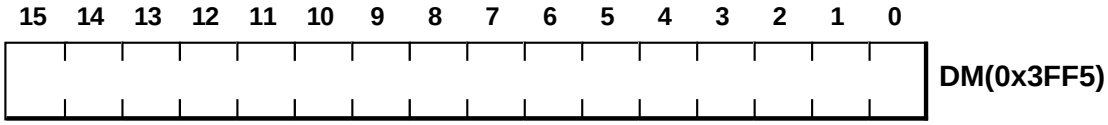
1 = channel enabled
0 = channel ignored

Memory-Mapped Registers

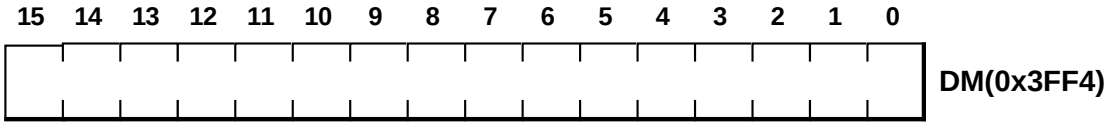
SPORT0 Autobuffer Control Register *(Not on ADSP-2105)*



SPORT0 SCLKDIV
Serial Clock Divide Modulus *(Not on ADSP-2105)*



SPORT0 RFSDIV
Receive Frame Sync Divide Modulus



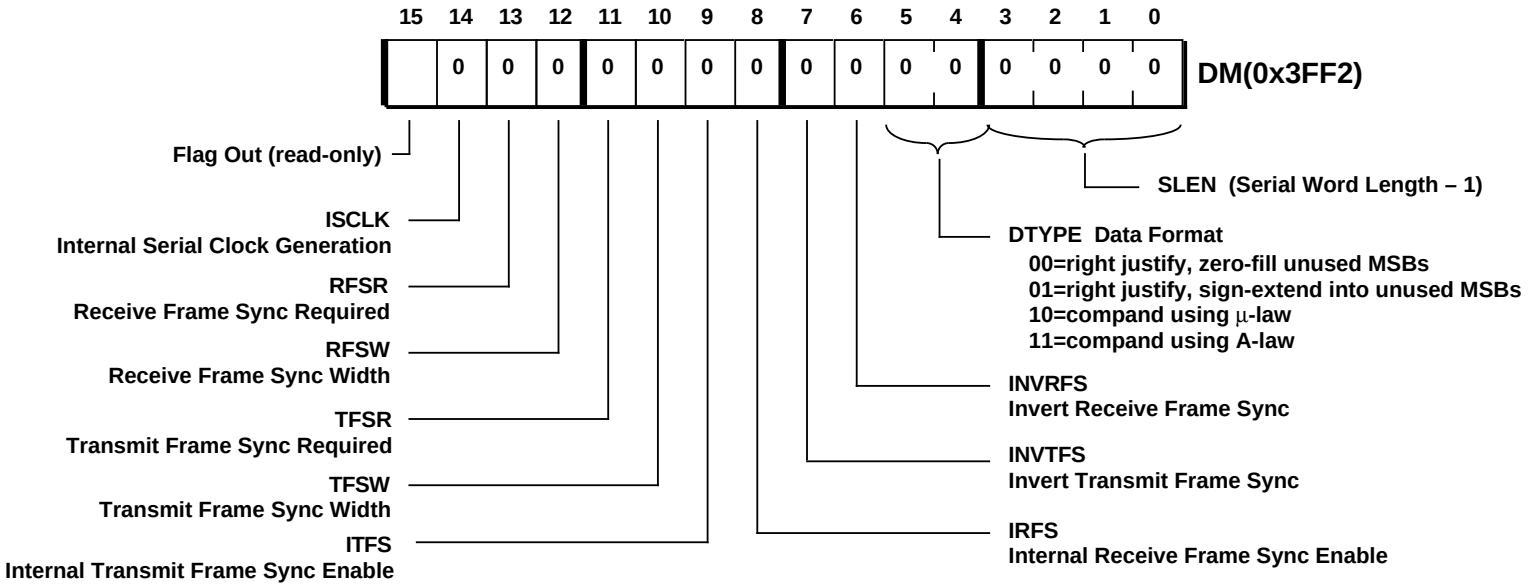
$$\text{SCLKDIV} = \frac{\text{CLKOUT frequency}}{2 * (\text{SCLK frequency})} - 1 \qquad \text{RFSDIV} = \frac{\text{SCLK frequency}}{\text{RFS frequency}} - 1$$

Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

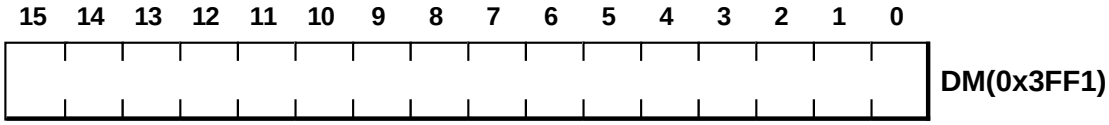
E Control/Status Registers

Memory-Mapped Registers

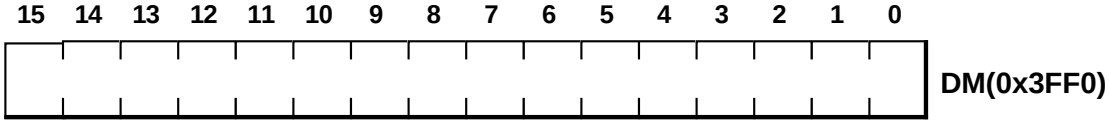
SPORT1 Control Register



SPORT1 SCLKDIV
Serial Clock Divide Modulus



SPORT1 RFSDIV
Receive Frame Sync Divide Modulus

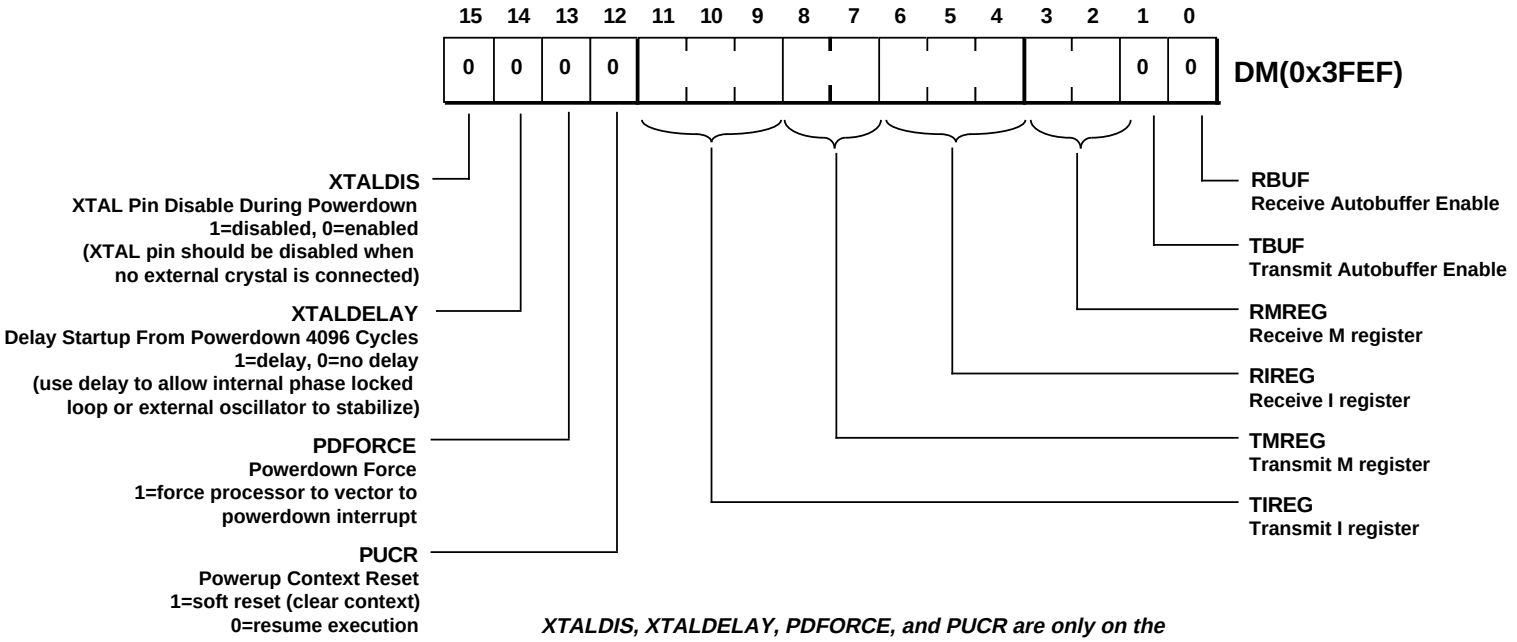


$$\text{SCLKDIV} = \frac{\text{CLKOUT frequency}}{2 * (\text{SCLK frequency})} - 1 \qquad \text{RFSDIV} = \frac{\text{SCLK frequency}}{\text{RFS frequency}} - 1$$

Control/Status Registers E

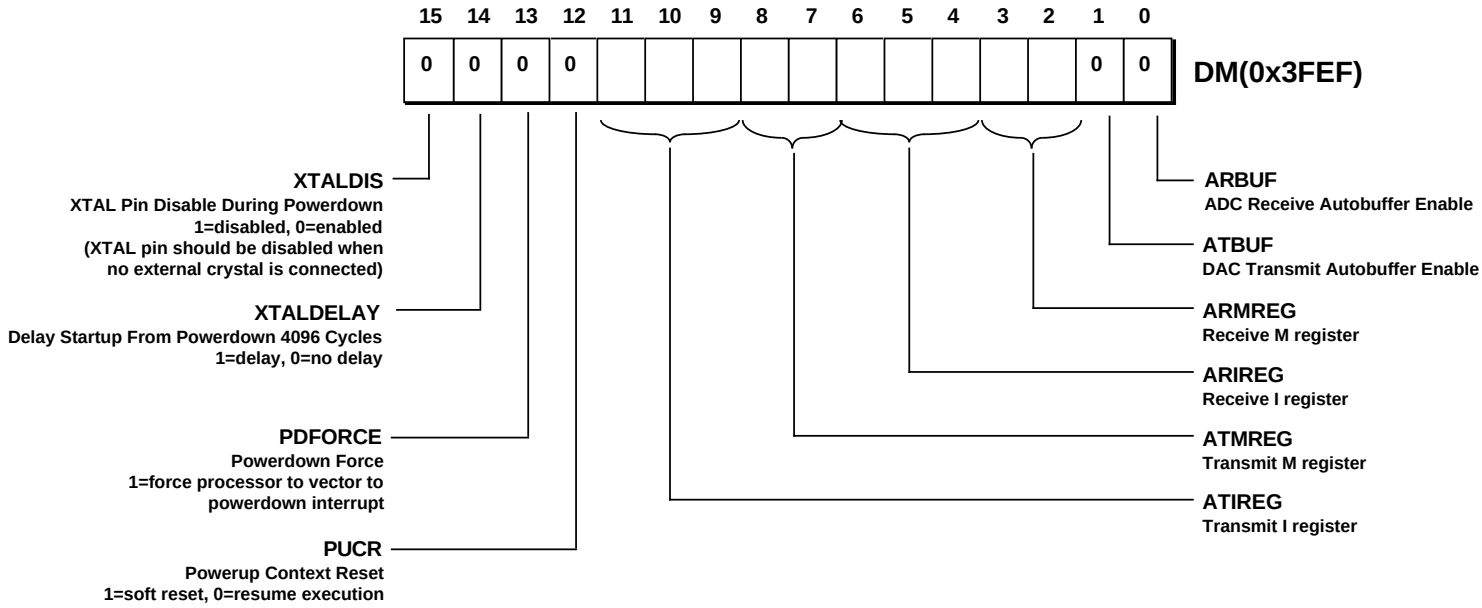
Memory-Mapped Registers

SPORT1 Autobuffer Control Register *(Not on ADSP-21msp5x)*



XTALDIS, XTALDELAY, PDFORCE, and PUCR are only on the ADSP-2171, ADSP-2181, and ADSP-21msp58/59 processors.

Analog Autobuffer Control Register *(ADSP-21msp5x only)*

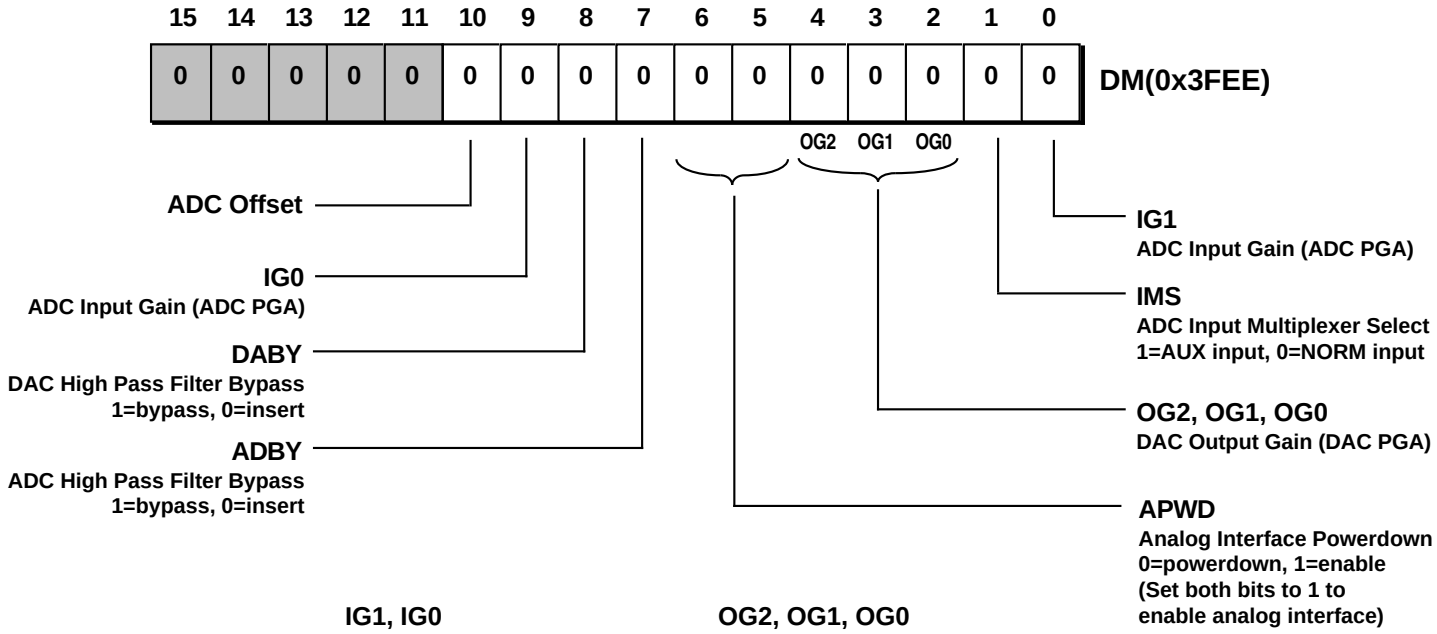


Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

E Control/Status Registers

Memory-Mapped Registers

Analog Control Register *(ADSP-21msp5x only)*



IG1, IG0
ADC Input Gain (ADC PGA)

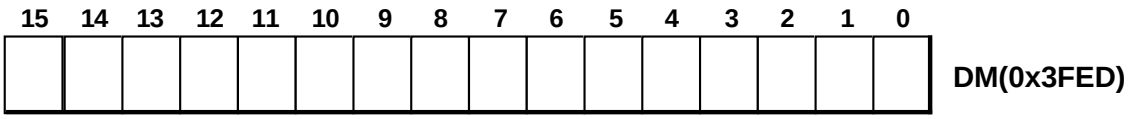
Gain	IG1	IG0
0 dB	0	0
+6 dB	0	1
+20 dB	1	0
+26 dB	1	1

OG2, OG1, OG0
DAC Output Gain (DAC PGA)

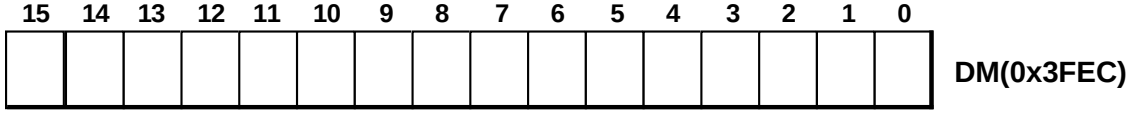
Gain	OG2	OG1	OG0
+6 dB	0	0	0
+3 dB	0	0	1
0 dB	0	1	0
–3 dB	0	1	1
–6 dB	1	0	0
–9 dB	1	0	1
–12 dB	1	1	0
–15 dB	1	1	1

Analog Data Registers *(ADSP-21msp5x only)*

ADC Receive Data

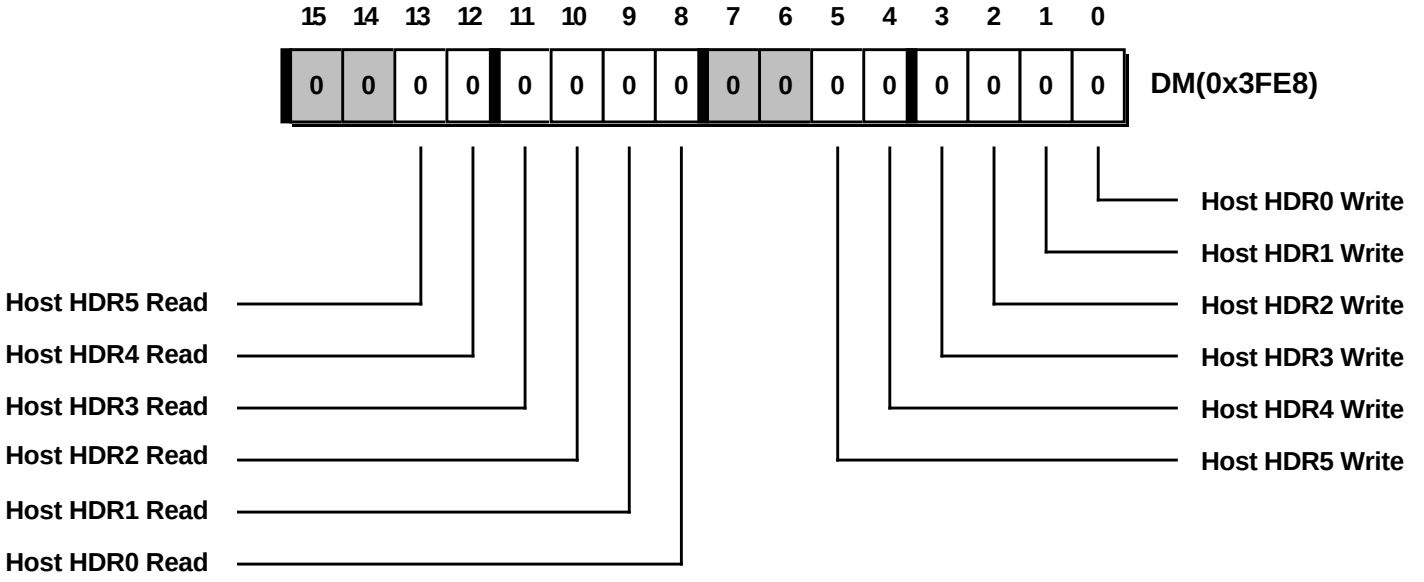


DAC Transmit Data

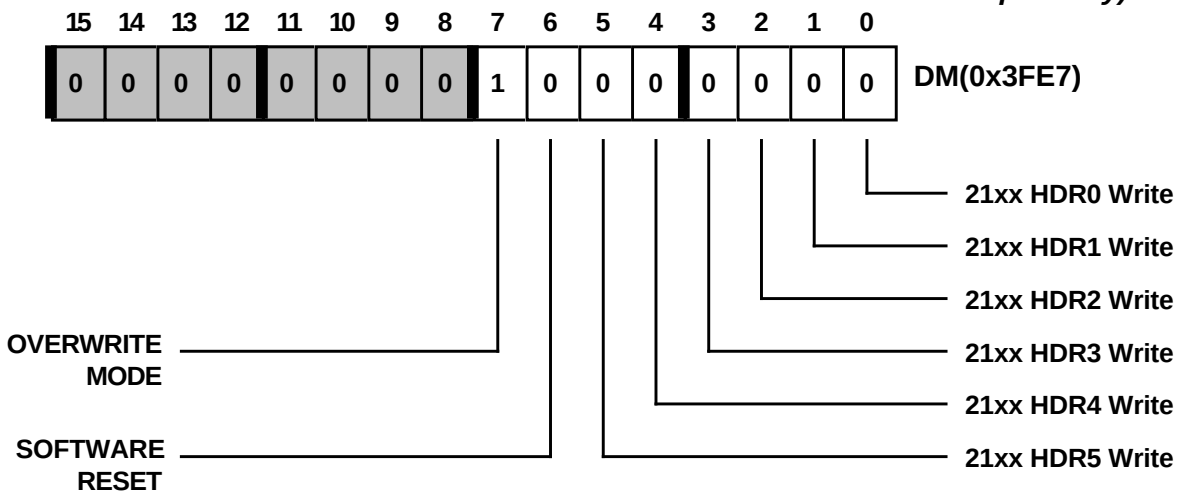


Memory-Mapped Registers

HMASK Interrupt Mask Register *(ADSP-2171, ADSP-2111, ADSP-21msp5x only)*



HSR7 Status Register *(ADSP-2171, ADSP-2111, ADSP-21msp5x only)*

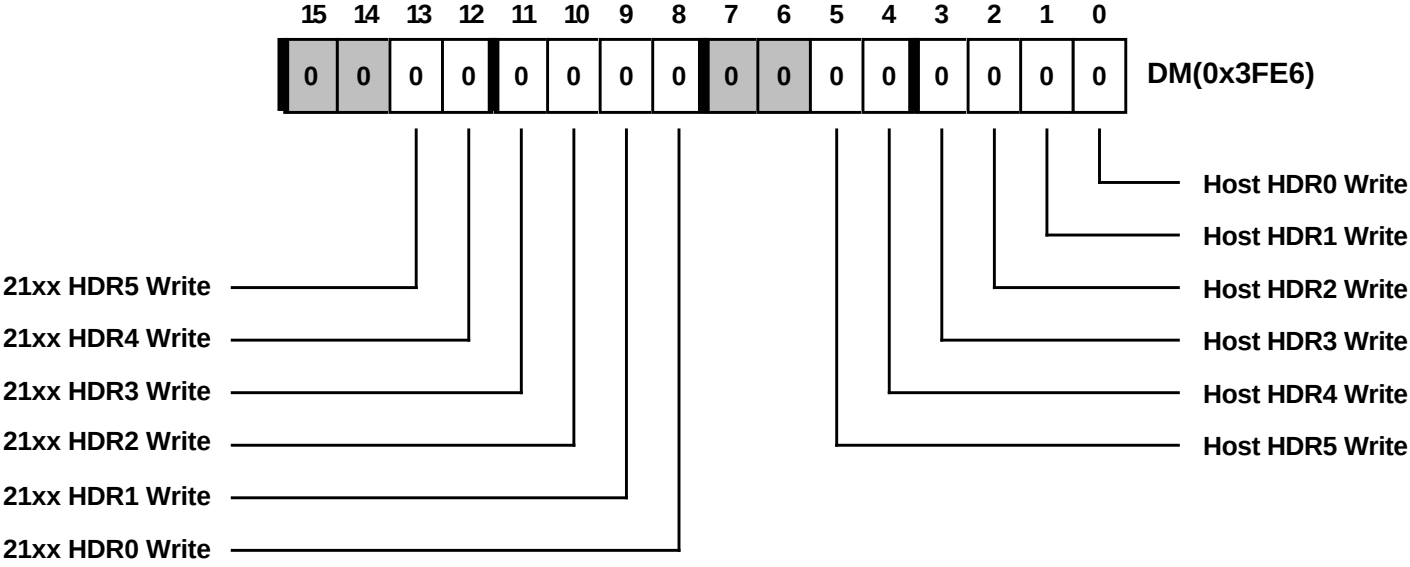


Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

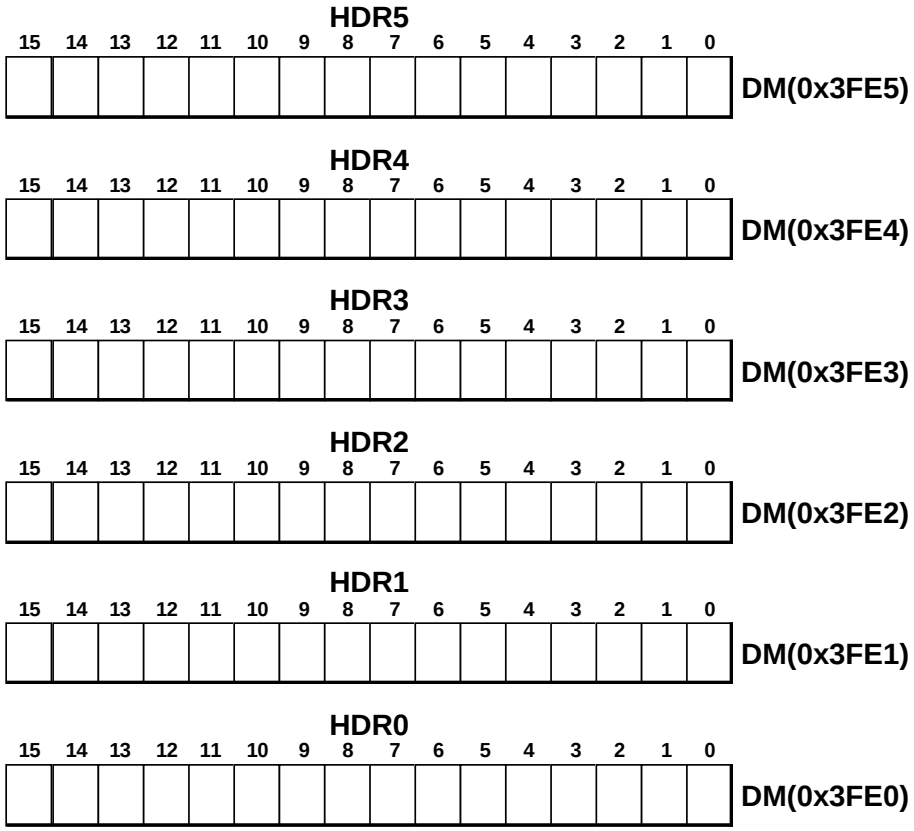
E Control/Status Registers

Memory-Mapped Registers

HSR6 Status Register *(ADSP-2171, ADSP-2111, ADSP-21msp5x only)*

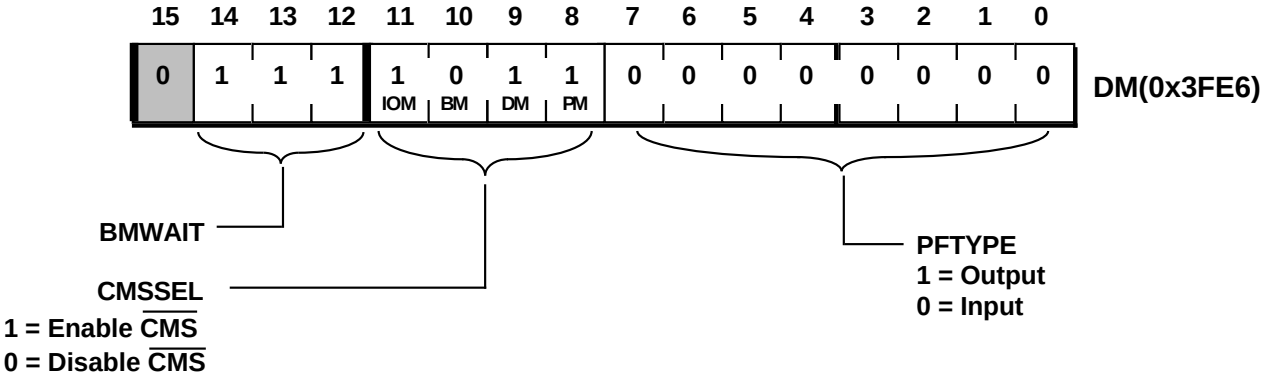


HIP Data Registers *(ADSP-2171, ADSP-2111, ADSP-21msp5x only)*

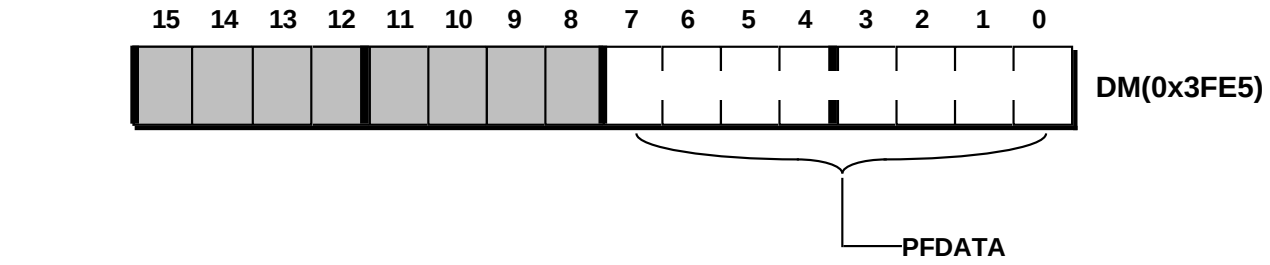


Memory-Mapped Registers

Programmable Flag & Composite Select Control ***(ADSP-2181 only)***



Programmable Flag Data ***(ADSP-2181 only)***

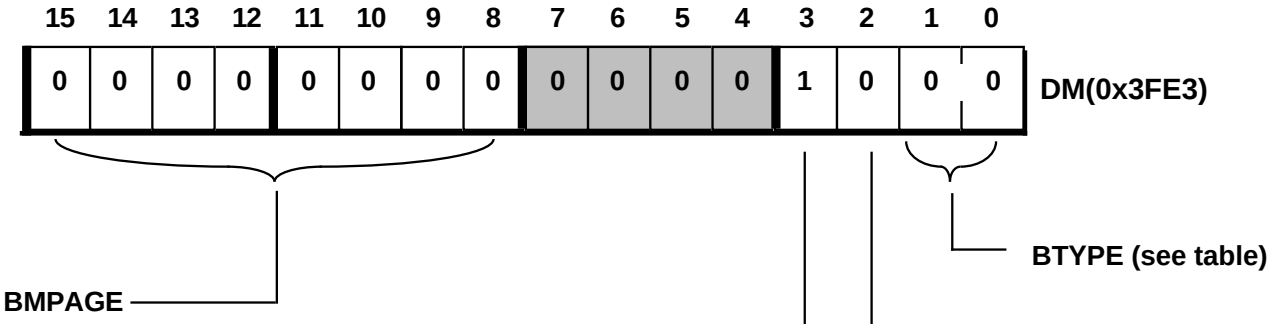


Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

E Control/Status Registers

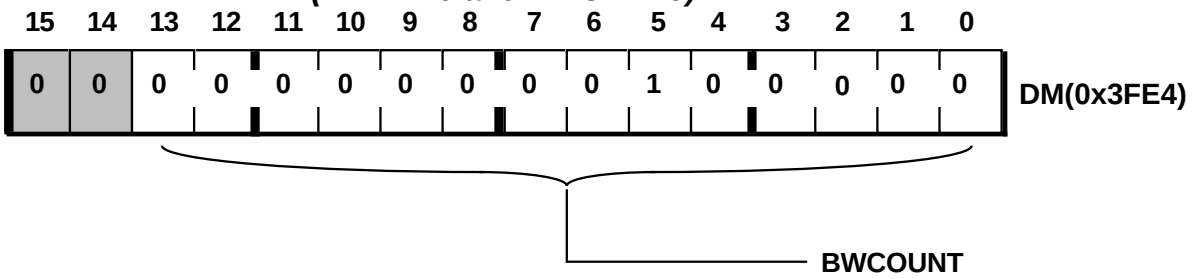
Memory-Mapped Registers

BDMA Control *(ADSP-2181 only)*



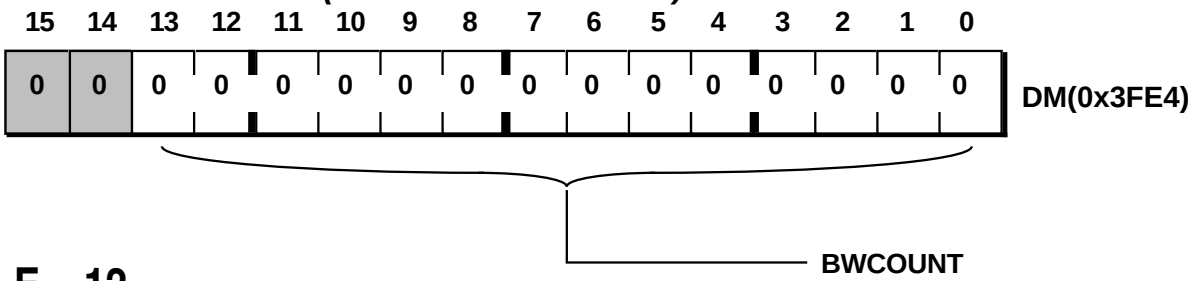
BTYPE	00	01	10	11
Internal Memory Space	PM	DM	DM	DM
Word Size	24	16	8	8
Alignment	full word	full word	MSB	LSB

BDMA Word Count *(ADSP-2181 only)*
(MMAP=0 and BMODE=0)



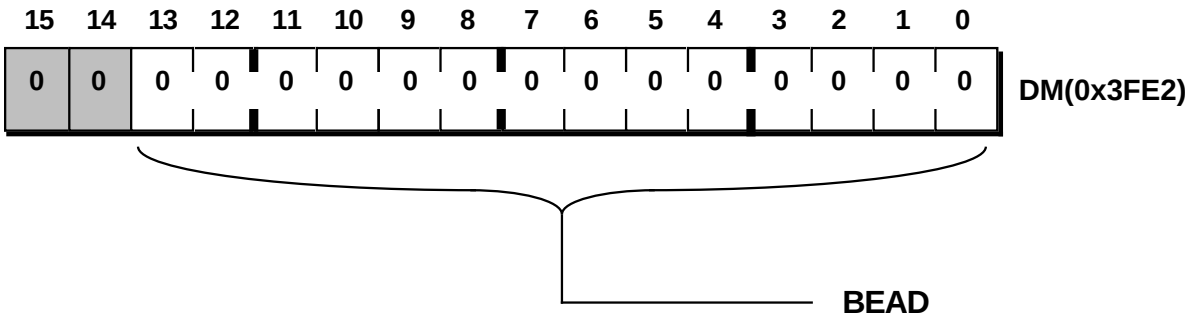
or

BDMA Word Count
(MMAP=1 or BMODE=1)

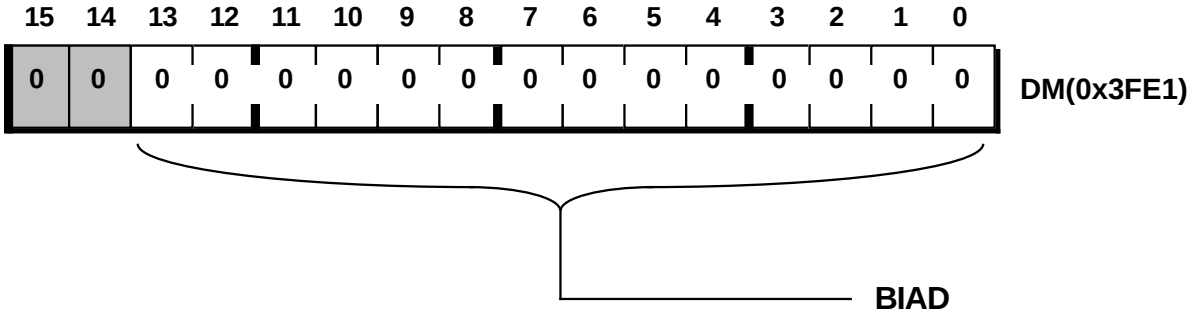


Memory-Mapped Registers

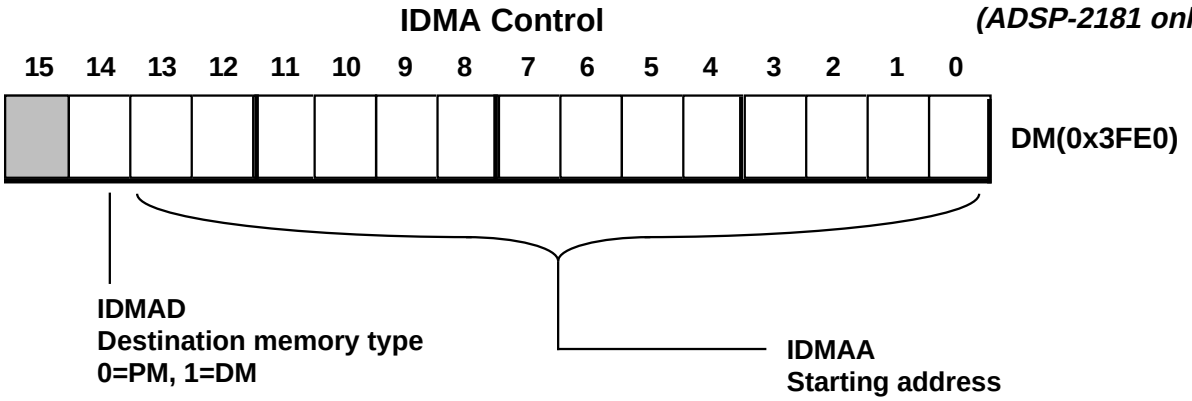
BDMA External Address *(ADSP-2181 only)*



BDMA Internal Address *(ADSP-2181 only)*



IDMA Control *(ADSP-2181 only)*

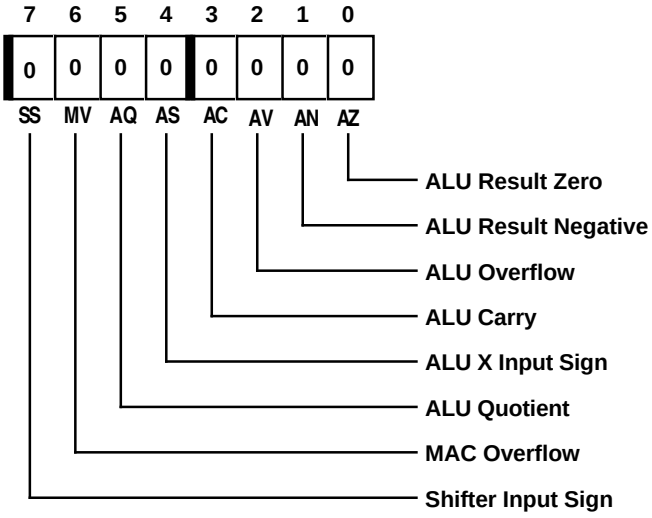


Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

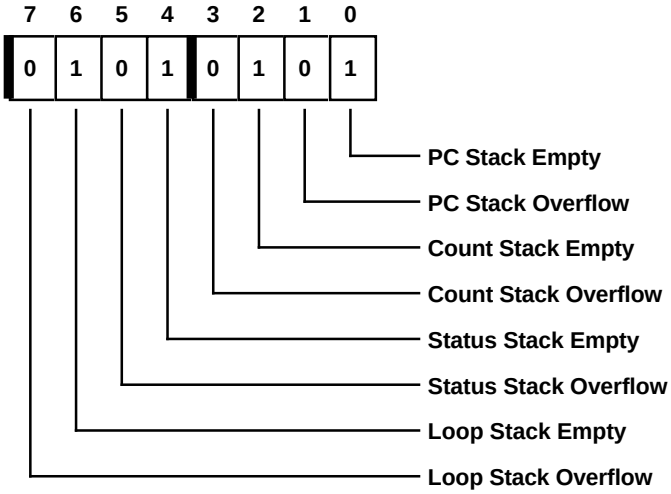
E Control/Status Registers

Non-Memory-Mapped Registers

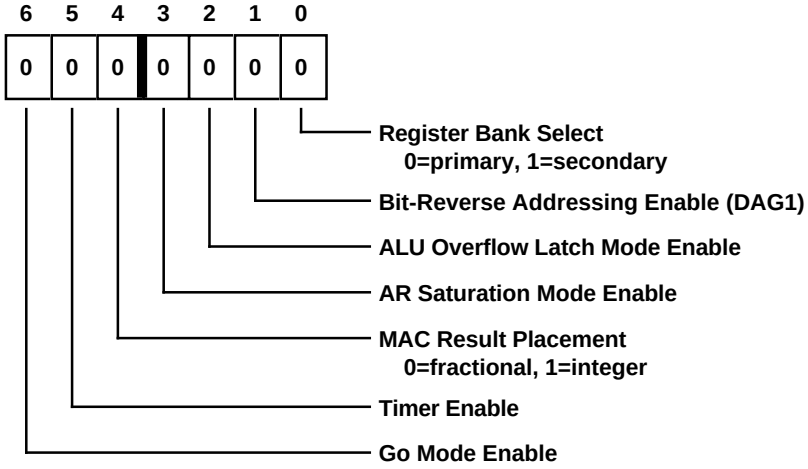
ASTAT



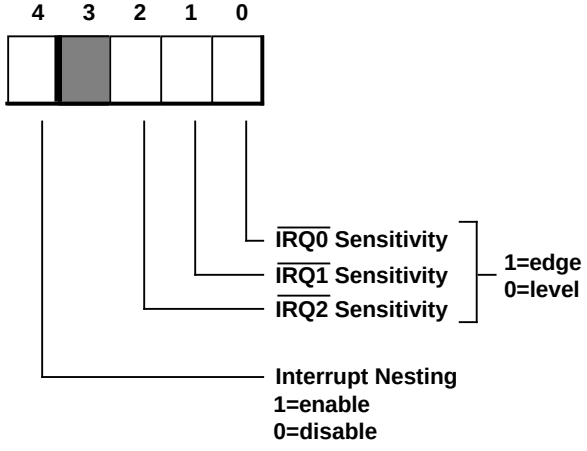
SSTAT *(read-only)*



MSTAT



ICNTL

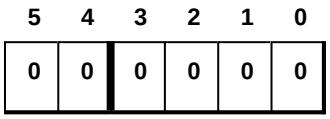


Control/Status Registers E

Non-Memory-Mapped Registers

ADSP-2101
ADSP-2105
ADSP-2115

IMASK



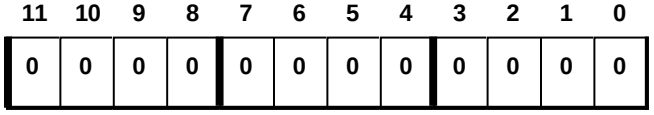
INTERRUPT ENABLES

1 = enable
0 = disable (mask)

Timer
SPORT1 Receive or $\overline{\text{IRQ0}}$
SPORT1 Transmit or $\overline{\text{IRQ1}}$
SPORT0 Receive ***(must be set to 0 for ADSP-2105)***
SPORT0 Transmit ***(must be set to 0 for ADSP-2105)***
$\overline{\text{IRQ2}}$

ADSP-2101
ADSP-2105
ADSP-2115
ADSP-2111

IFC ***(write-only)***



INTERRUPT FORCE BITS

$\overline{\text{IRQ2}}$
SPORT0 Transmit
(must be set to 0 for ADSP-2105)
SPORT0 Receive
(must be set to 0 for ADSP-2105)
SPORT1 Transmit or $\overline{\text{IRQ1}}$
SPORT1 Receive or $\overline{\text{IRQ0}}$
Timer

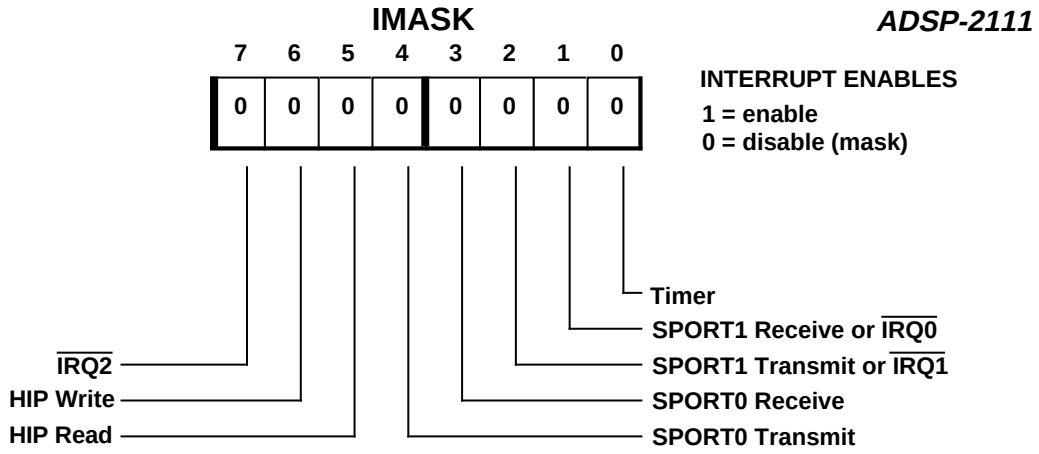
INTERRUPT CLEAR BITS

Timer
SPORT1 Receive or $\overline{\text{IRQ0}}$
SPORT1 Transmit or $\overline{\text{IRQ1}}$
SPORT0 Receive
(must be set to 0 for ADSP-2105)
SPORT0 Transmit
(must be set to 0 for ADSP-2105)
$\overline{\text{IRQ2}}$

Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

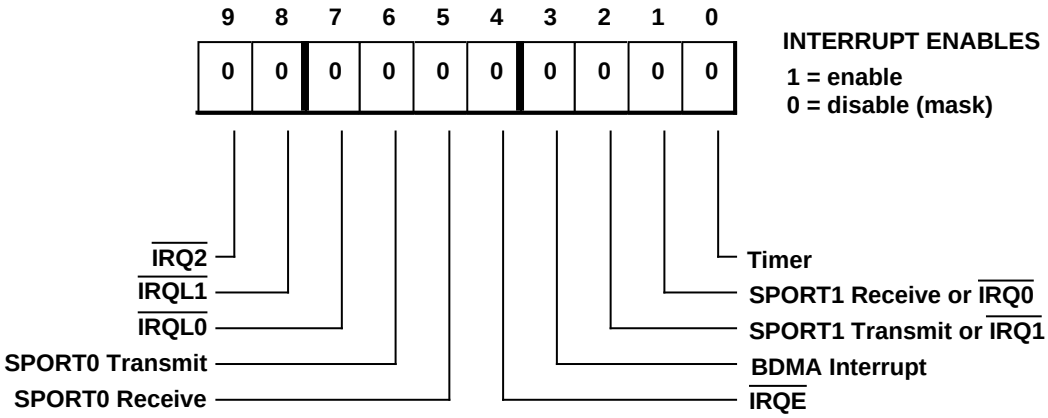
E Control/Status Registers

Non-Memory-Mapped Registers

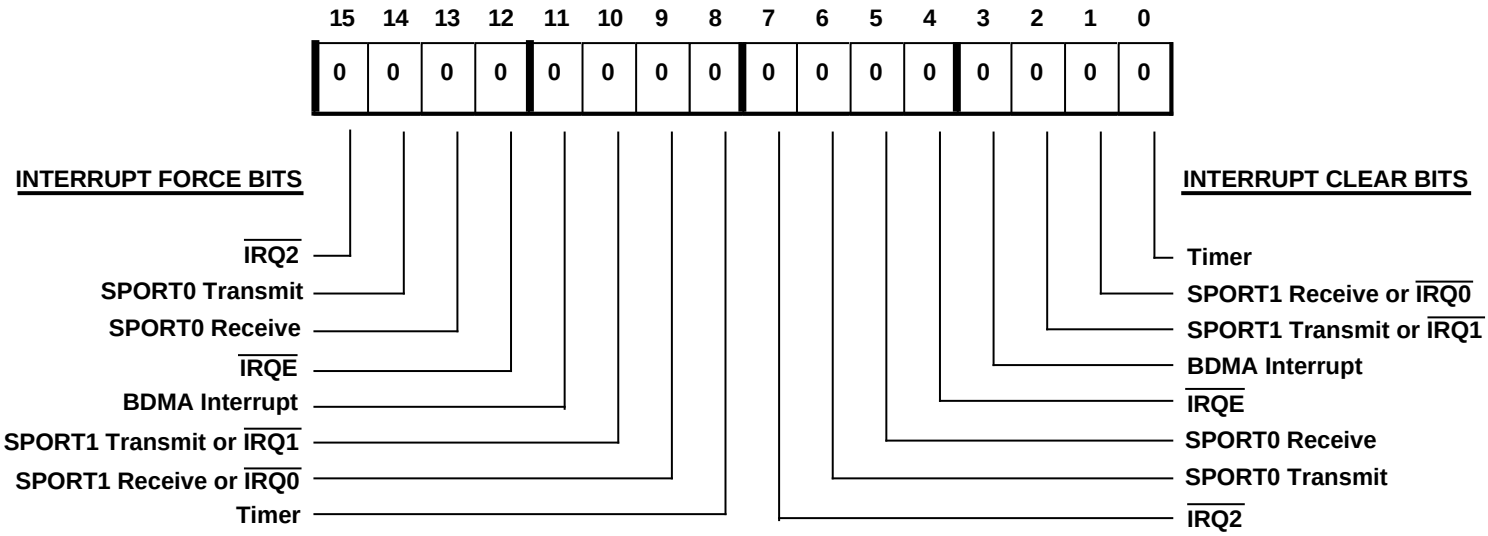


Non-Memory-Mapped Registers

IMASK *ADSP-2181*



IFC *(write-only)* *ADSP-2181*

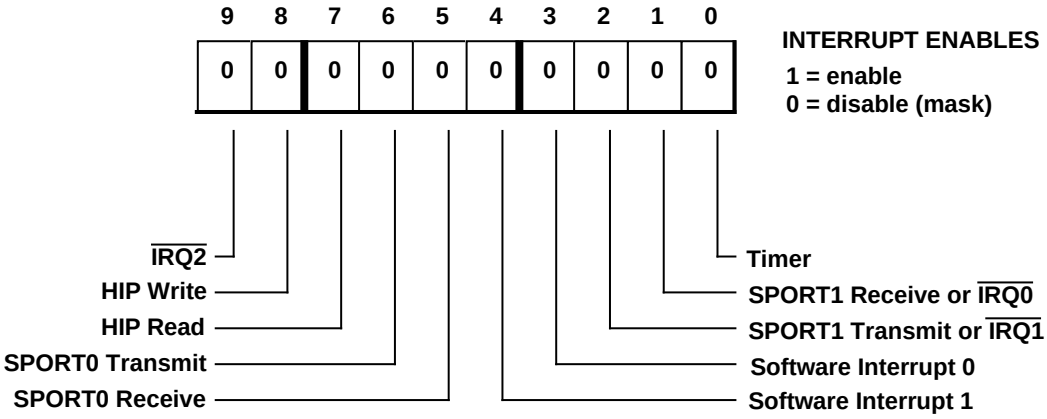


Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

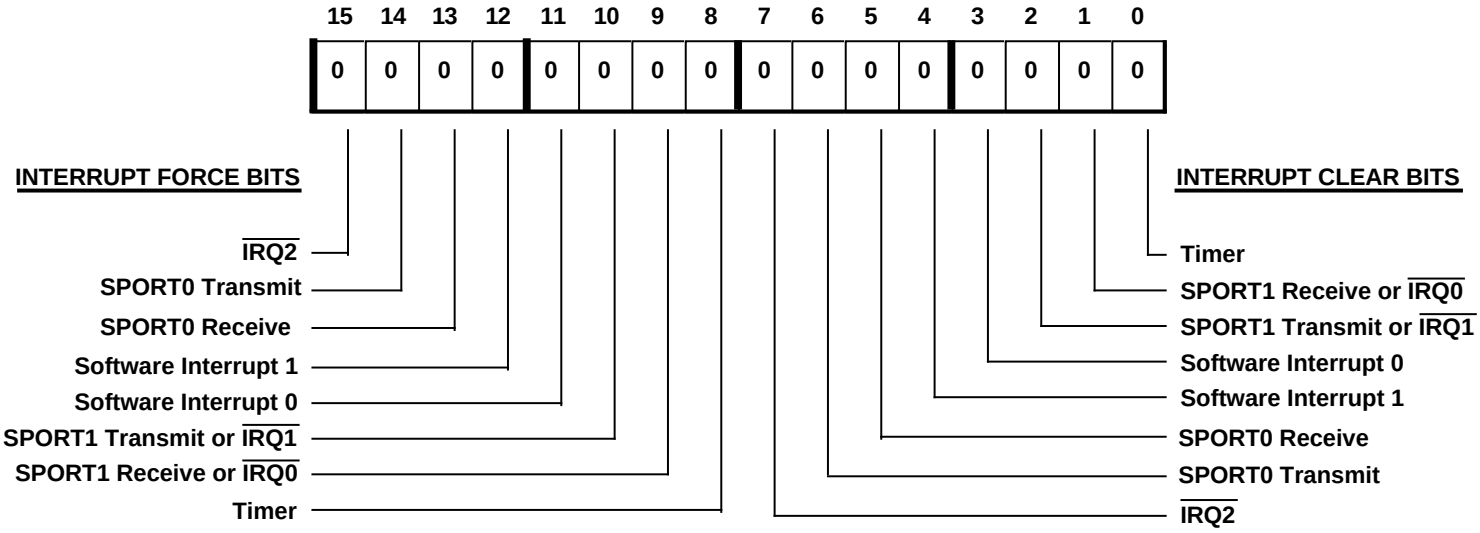
E Control/Status Registers

Non-Memory-Mapped Registers

IMASK ***ADSP-2171***



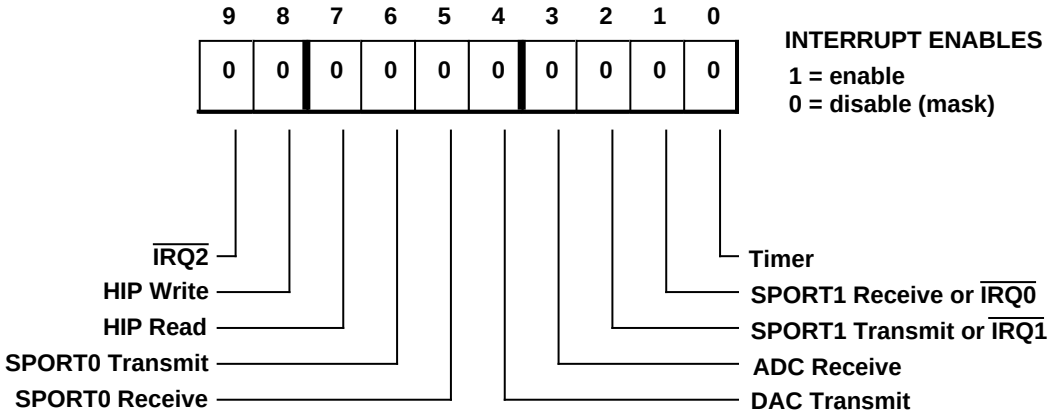
IFC *(write-only)* ***ADSP-2171***



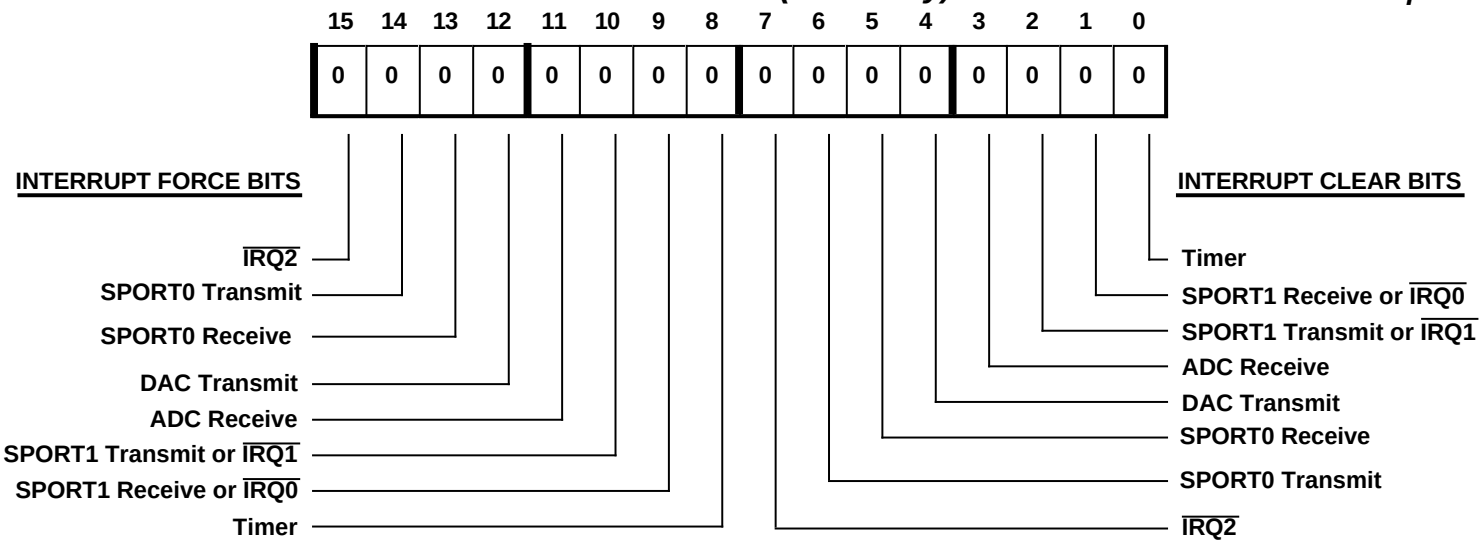
Control/Status Registers E

Non-Memory-Mapped Registers

IMASK *ADSP-21msp5x*



IFC *(write-only)* *ADSP-21msp5x*



Default bit values at reset are shown; if no value is shown, the bit is undefined at reset.
Reserved bits are shown on a gray field—these bits should always be written with zeros.

E Control/Status Registers