Interrupt Vector Addresses D

D.1 INTERRUPT VECTOR ADDRESSES

Tables D.1–D.6 show the interrupts and associated vector addresses for each processor of the ADSP-2100 family. Note that SPORT1 can be configured as either a serial port or as a collection of control pins including two external interrupt inputs, $\overline{IRQ0}$ and $\overline{IRQ1}$.

The interrupt vector locations are spaced four program memory locations apart—this allows short interrupt service routines to be coded in place, with no jump to the service routine required. For interrupt service routines with more than four instructions, however, program control must be transferred to the service routine by means of a jump instruction placed at the interrupt vector location.

Interrupt Source	*Interrupt Vector Address*
$\overline{RESET}$ startup	0x0000
$\overline{IRQ2}$	0x0004 *(highest priority)*
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit *or* $\overline{IRQ1}$	0x0010
SPORT1 Receive *or* $\overline{IRQ0}$	0x0014
Timer	0x0018 *(lowest priority)*

Table D.1 ADSP-2101/2115 Interrupts & Interrupt Vector Addresses

Interrupt Source	*Interrupt Vector Address*
$\overline{RESET}$ startup	0x0000
$\overline{IRQ2}$	0x0004 *(highest priority)*
SPORT1 Transmit *or* $\overline{IRQ1}$	0x0010
SPORT1 Receive *or* $\overline{IRQ0}$	0x0014
Timer	0x0018 *(lowest priority)*

Table D.2 ADSP-2105 Interrupts & Interrupt Vector Addresses

D Interrupt Vector Addresses

Interrupt Source	*Interrupt Vector Address*
$\overline{\text{RESET}}$ startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(highest priority)*
HIP Write (from Host)	0x0008
HIP Read (to Host)	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0018
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x001C
Timer	0x0020 *(lowest priority)*

Table D.3 ADSP-2111 Interrupts & Interrupt Vector Addresses

Interrupt Source	*Interrupt Vector Address*
$\overline{\text{RESET}}$ startup (or powerup w/PUCR=1)	0x0000 *(highest priority)*
Powerdown (non-maskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
HIP Write (from Host)	0x0008
HIP Read (to Host)	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
Software Interrupt 1	0x0018
Software Interrupt 2	0x001C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 *(lowest priority)*

Table D.4 ADSP-2171 Interrupts & Interrupt Vector Addresses

Interrupt Source	*Interrupt Vector Address*
$\overline{\text{RESET}}$ startup (or powerup w/PUCR=1)	0x0000 *(highest priority)*
Powerdown (non-maskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$ (level-sensitive)	0x0008
$\overline{\text{IRQL0}}$ (level-sensitive)	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$ (edge-sensitive)	0x0018
Byte DMA (BDMA) Interrupt	0x001C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 *(lowest priority)*

Table D.5 ADSP-2181 Interrupts & Interrupt Vector Addresses

Interrupt Vector Addresses D

Interrupt Source	*Interrupt Vector Address*
$\overline{\text{RESET}}$ startup (or powerup w/PUCR=1)	0x0000 *(highest priority)*
Powerdown (non-maskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
HIP Write (from Host)	0x0008
HIP Read (to Host)	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
Analog (DAC) Transmit	0x0018
Analog (ADC) Receive	0x001C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 *(lowest priority)*

Table D.6 ADSP-21msp58/59 Interrupts & Interrupt Vector Addresses