B CONTROL/STATUS REGISTERS

Overview

This appendix shows bit definitions for ADSP-218x memory-mapped control registers and non-memory-mapped control and status registers. The memory-mapped registers are listed in descending address order. Default bit values at reset are shown. If no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These reserved bits must be set to zero.

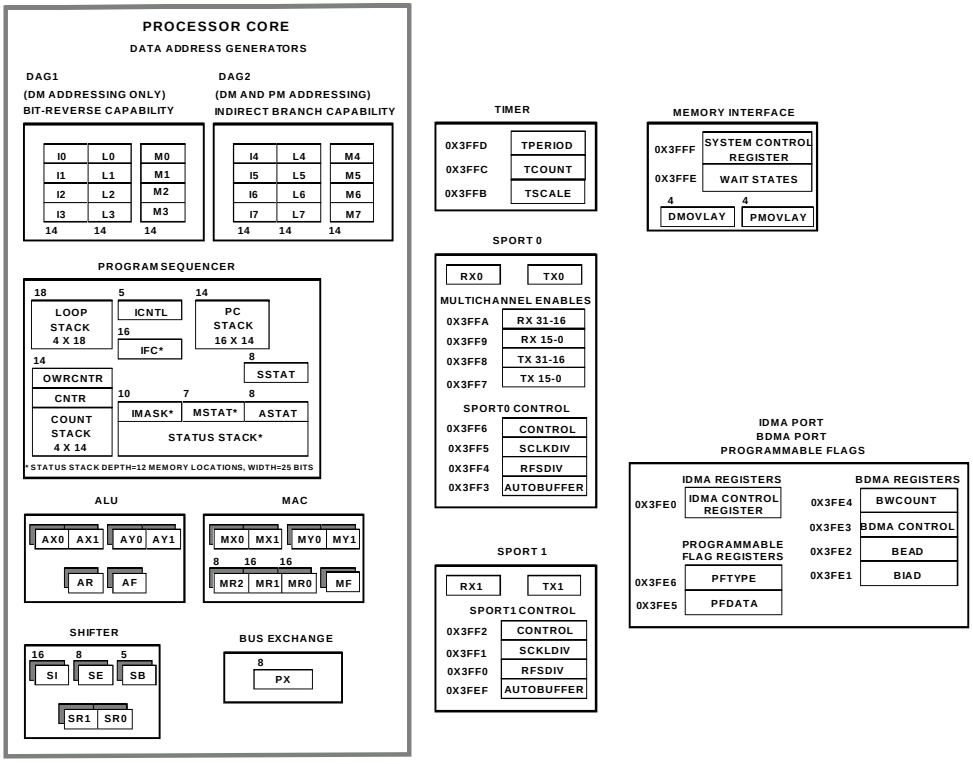


Figure B-1. ADSP-218x Registers

Memory-Mapped Registers

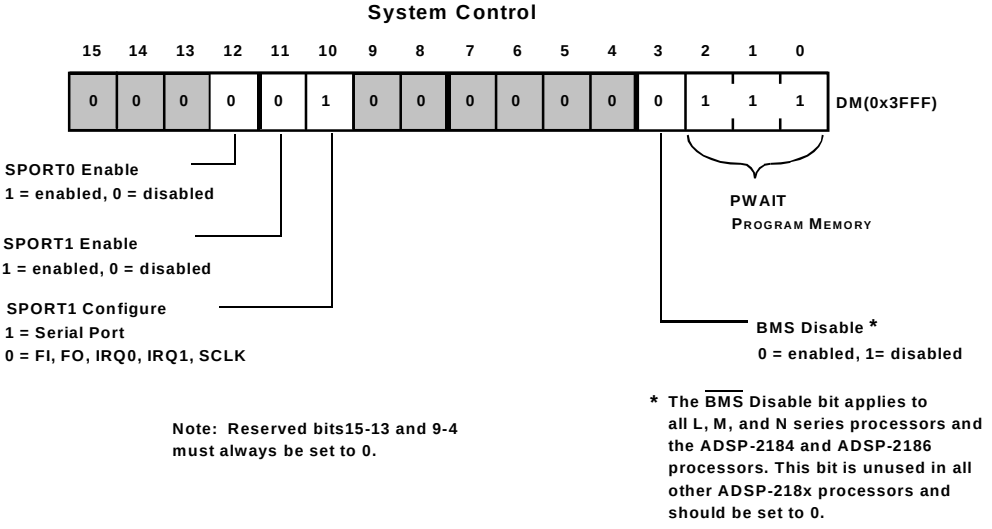


Figure B-2. System Control Register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

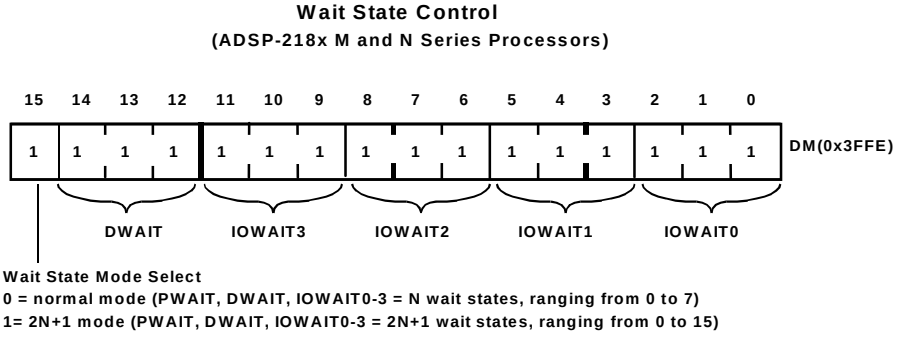


Figure B-3. Wait State Control Register (ADSP-218x M and N Series)

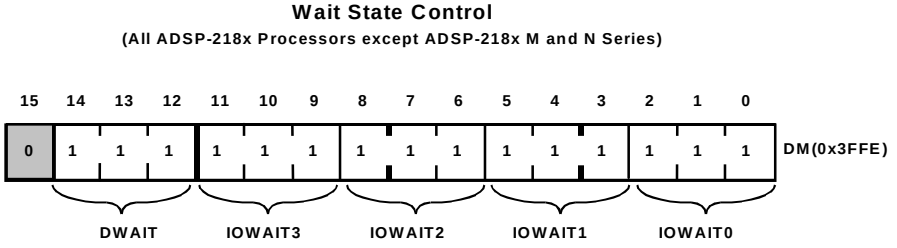


Figure B-4. Wait State Control Register (All ADSP-218x Processors except the M and N Series)

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

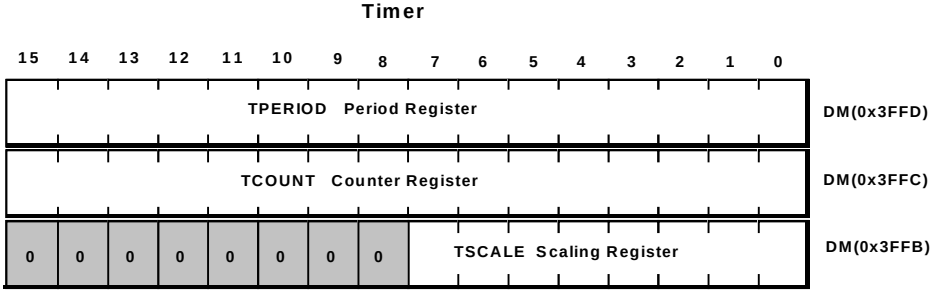


Figure B-5. Timer Registers

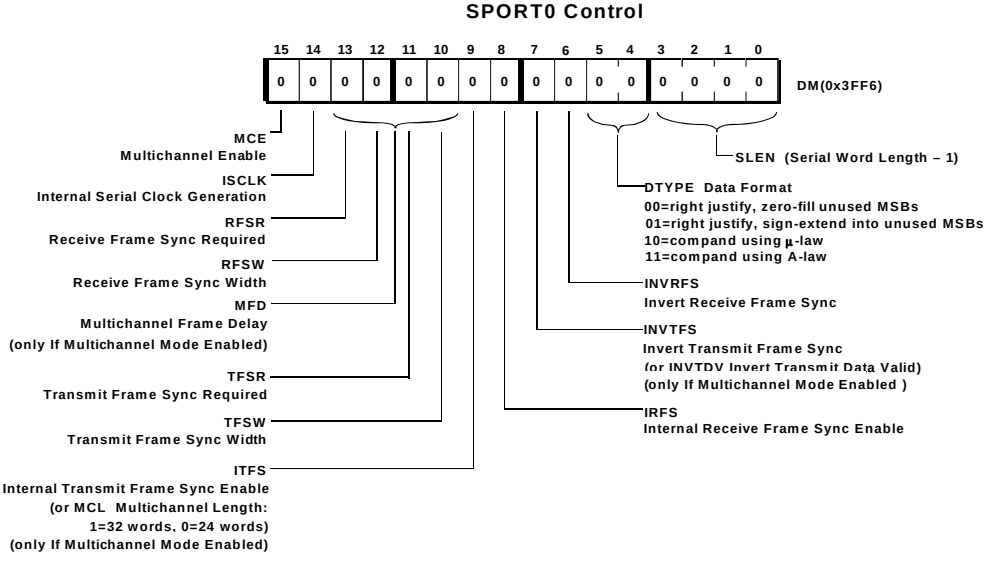


Figure B-6. SPORT0 Control Register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These reserved bits must be set to zero.

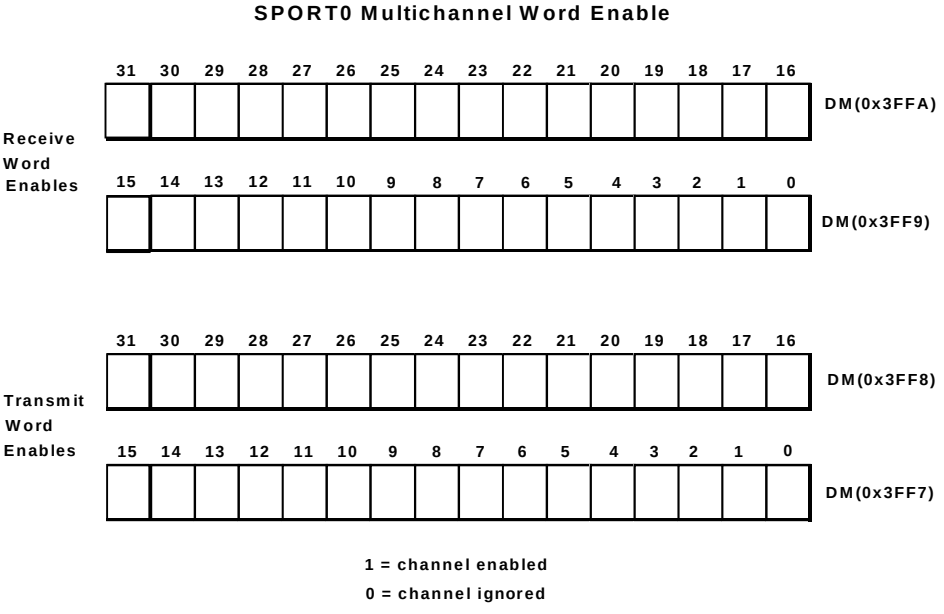


Figure B-7. SPORT0 Multichannel Word Enable Registers

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

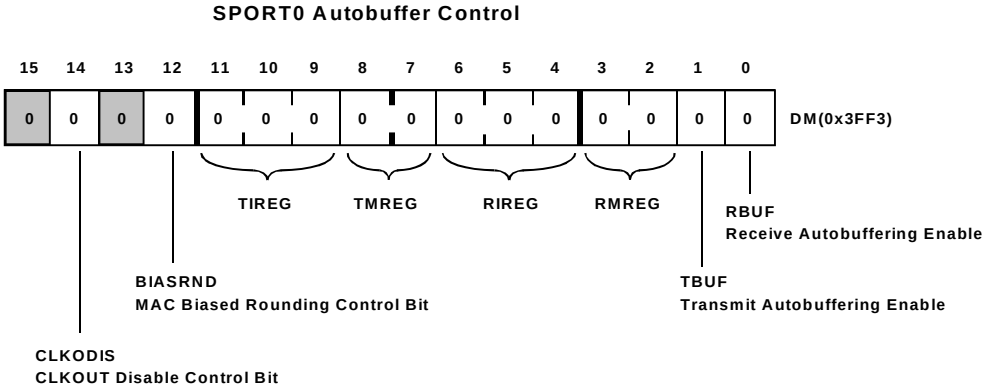


Figure B-8. SPORT0 Autobuffer Control Register

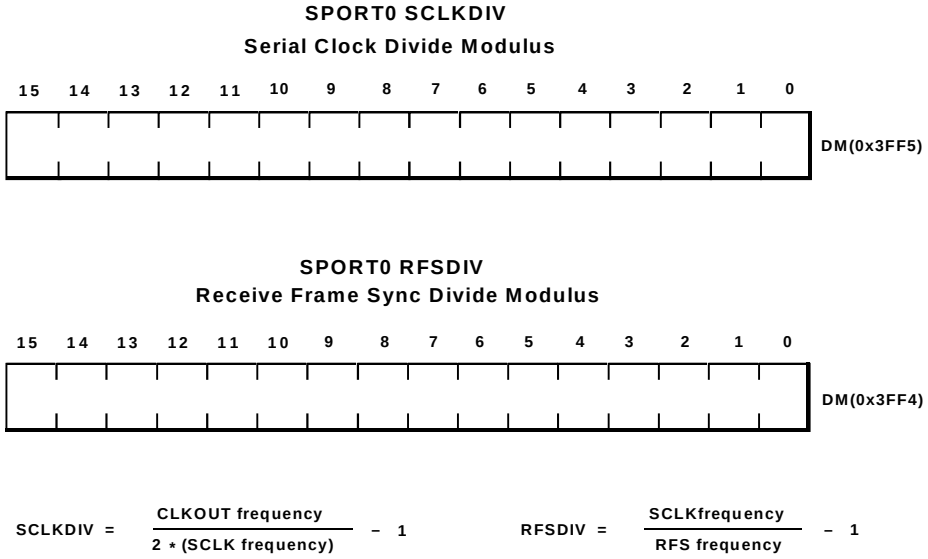


Figure B-9. SPORT0 SCLKDIV and RFSDIV Registers

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These reserved bits must be set to zero.

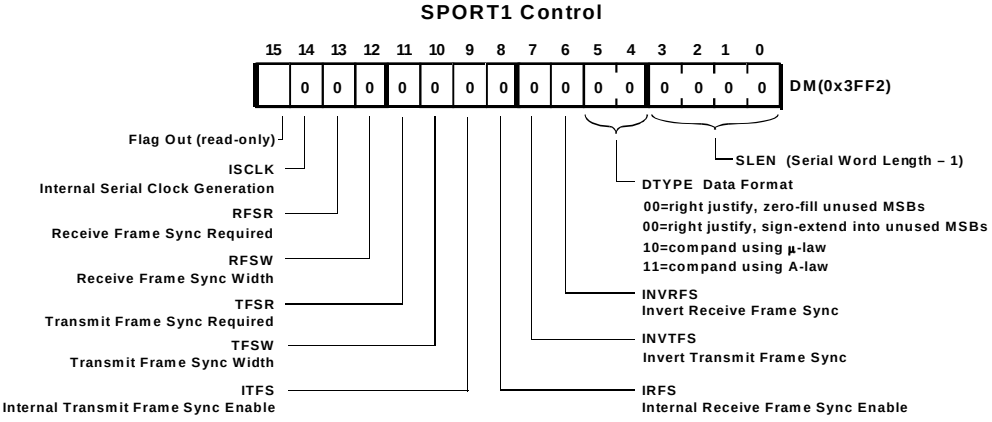


Figure B-10. SPORT1 Control register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

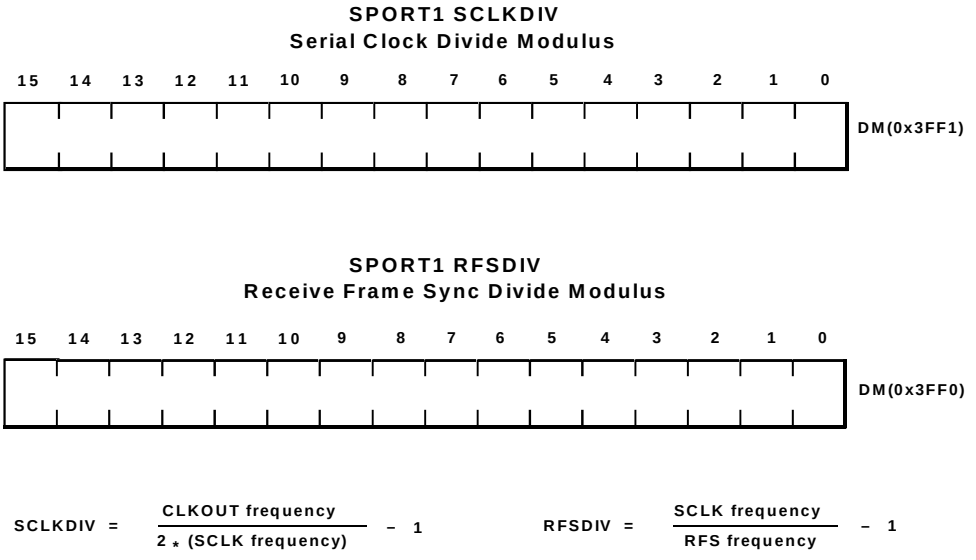


Figure B-11. SPORT1 SCLKDIV and RFSDIV Registers

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

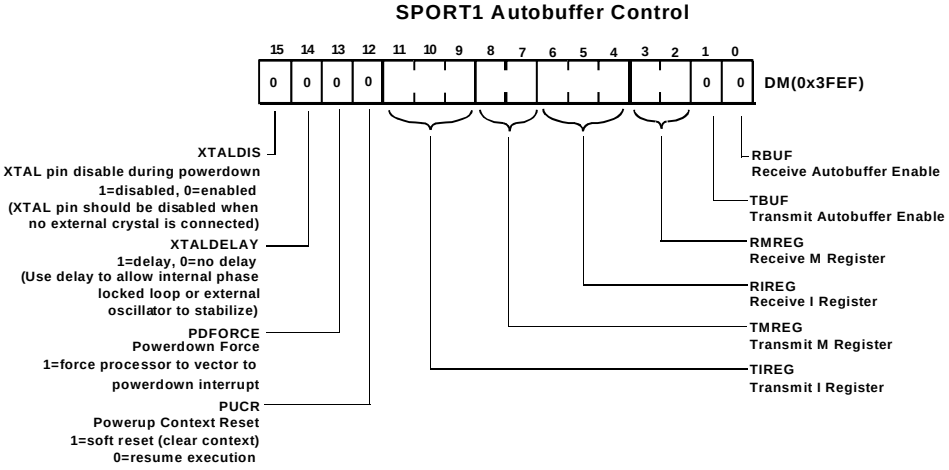


Figure B-12. SPORT1 Autobuffer Control Register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

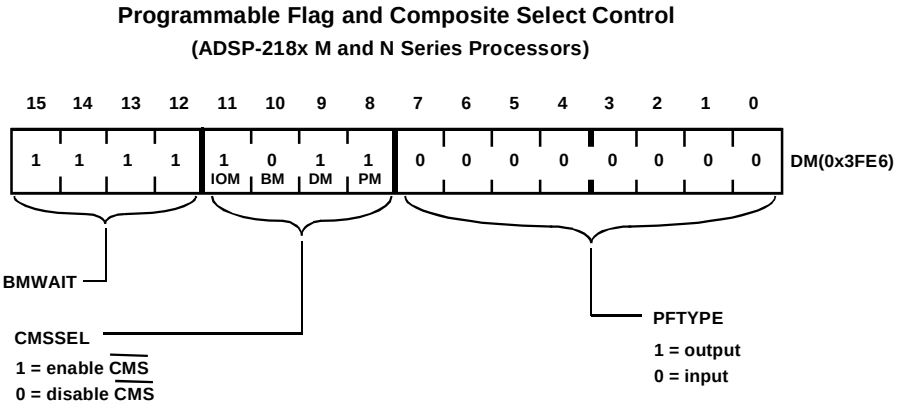


Figure B-13. Programmable Flag and Composite Select Control Register (ADSP-218x M and N Series Processors)

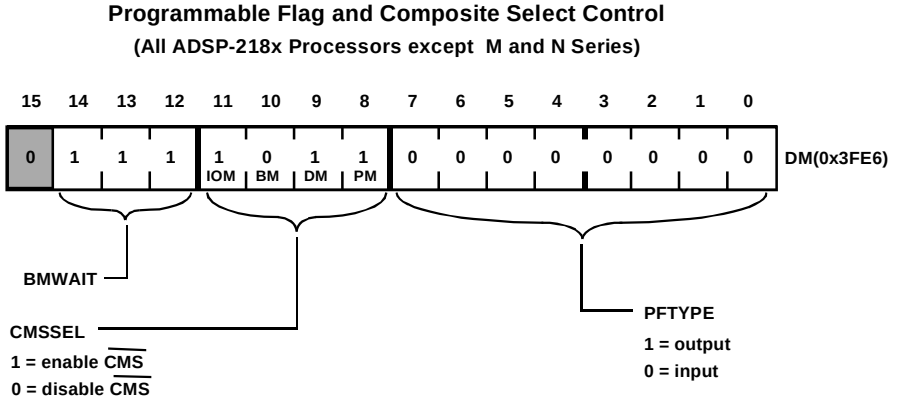


Figure B-14. Programmable Flag and Composite Select Control Register (All ADSP-218x processors except M and N Series)

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

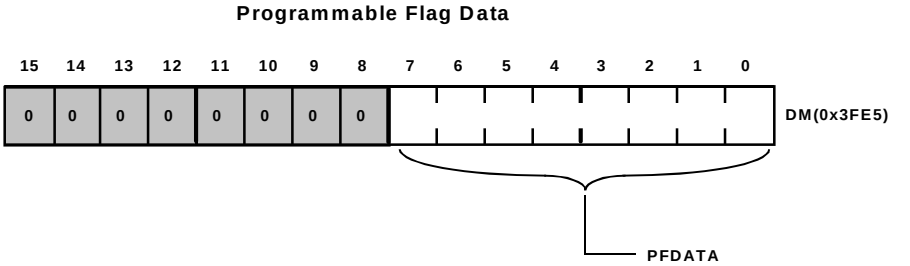


Figure B-15. Programmable Flag Data Register

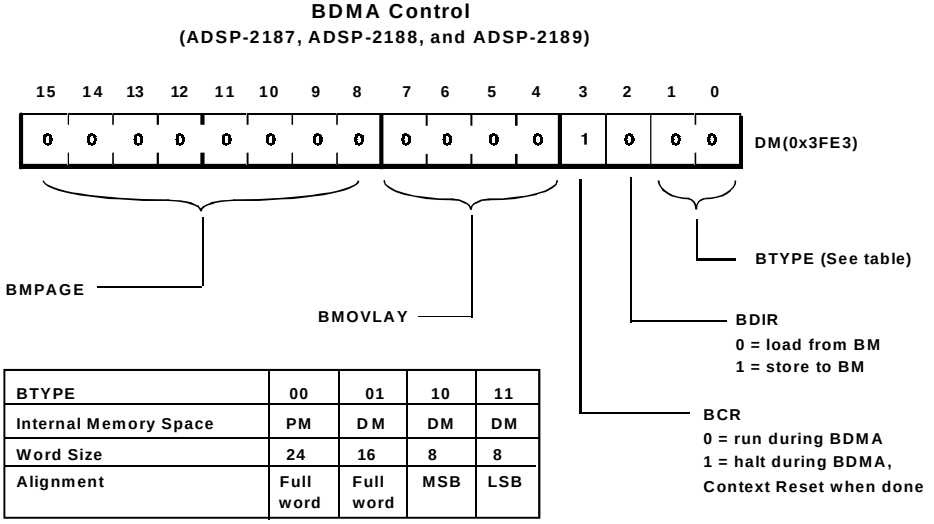
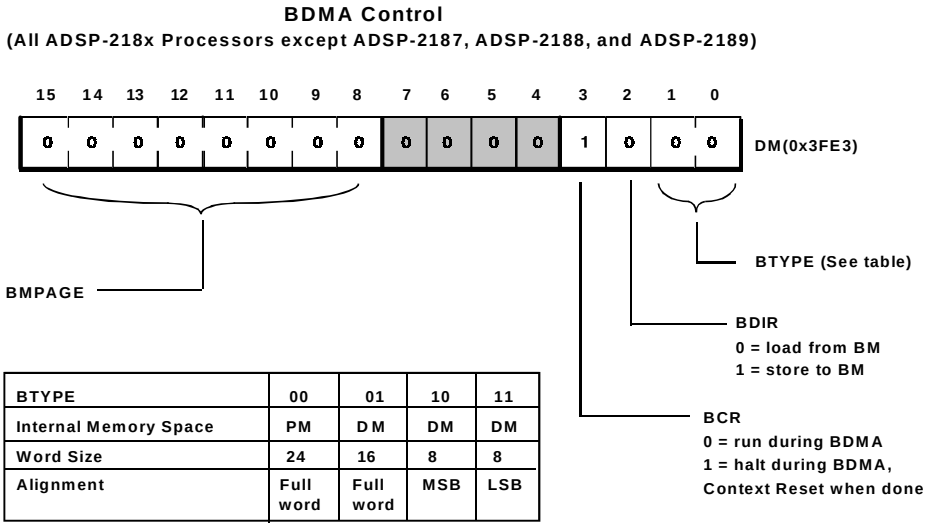


Figure B-16. BDMA Control Register (All ADSP-2187, ADSP-2188, ADSP-2189 Processors)

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These reserved bits must be set to zero.



BTYPE	00	01	10	11
Internal Memory Space	PM	DM	DM	DM
Word Size	24	16	8	8
Alignment	Full word	Full word	MSB	LSB

Figure B-17. BDMA Control Register (All ADSP-218x Processors except ADSP-2187, ADSP-2188, and ADSP-2189)

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These reserved bits must be set to zero.

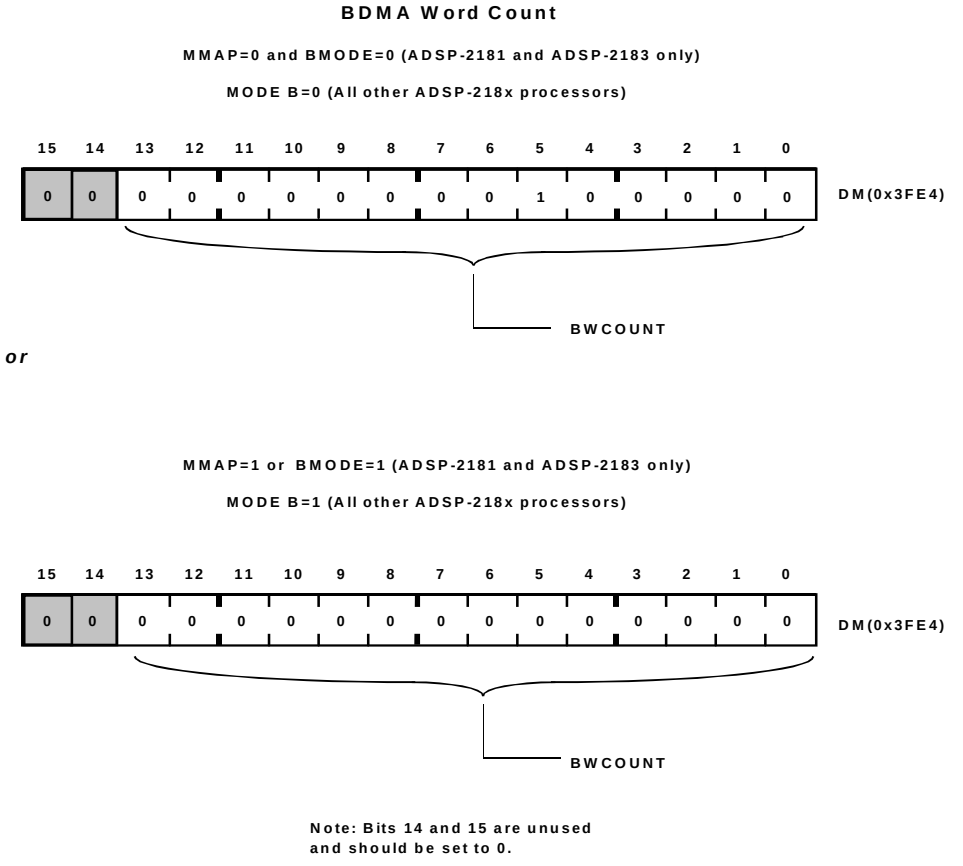


Figure B-18. BDMA Word Count Register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

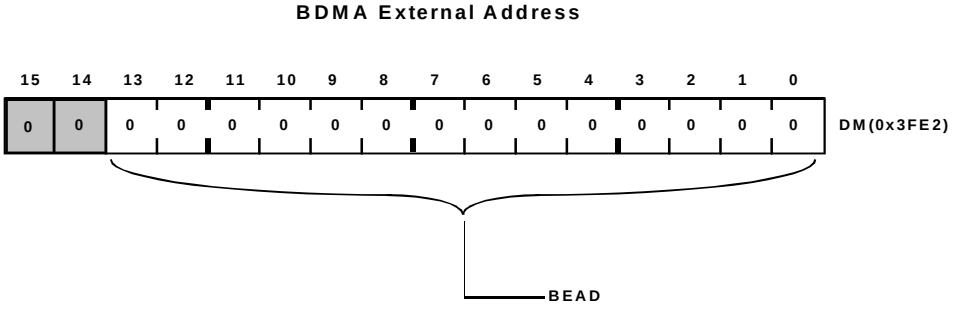


Figure B-19. BDMA External Address Register

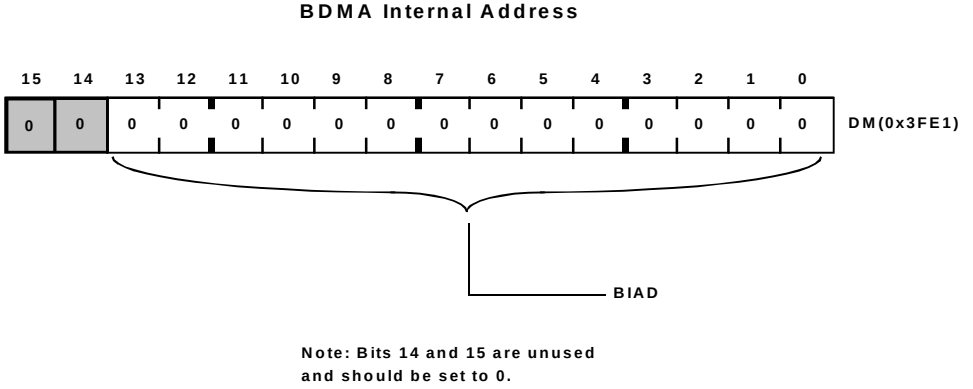


Figure B-20. BDMA Internal Address Register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

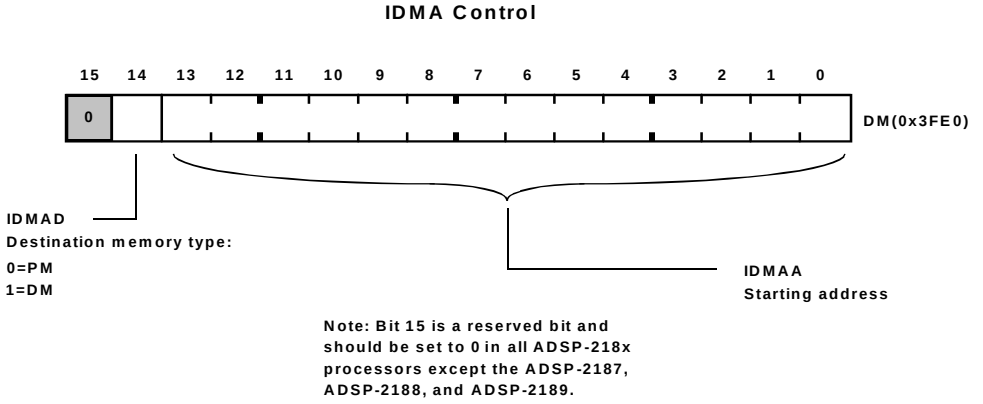


Figure B-21. IDMA Control Register

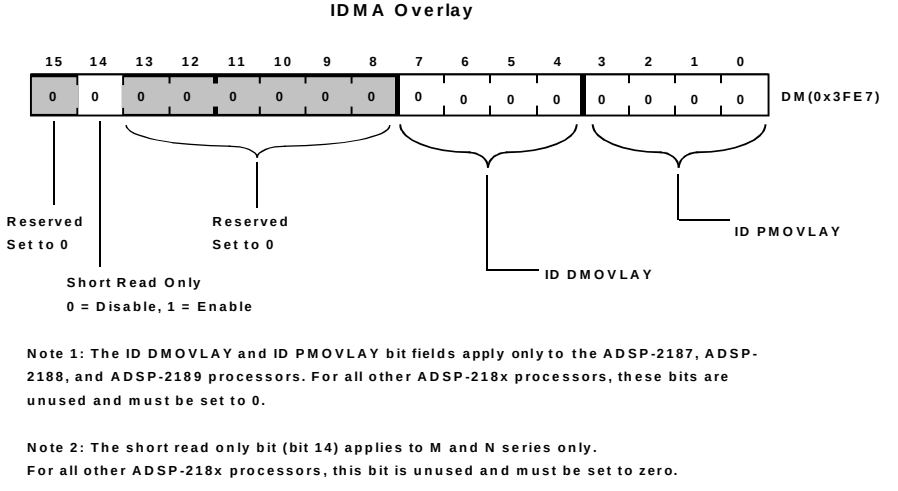


Figure B-22. IDMA Overlay Register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset.
Reserved bits are shown on a grey field. These reserved bits must be set to zero.

Non-Memory Mapped Registers

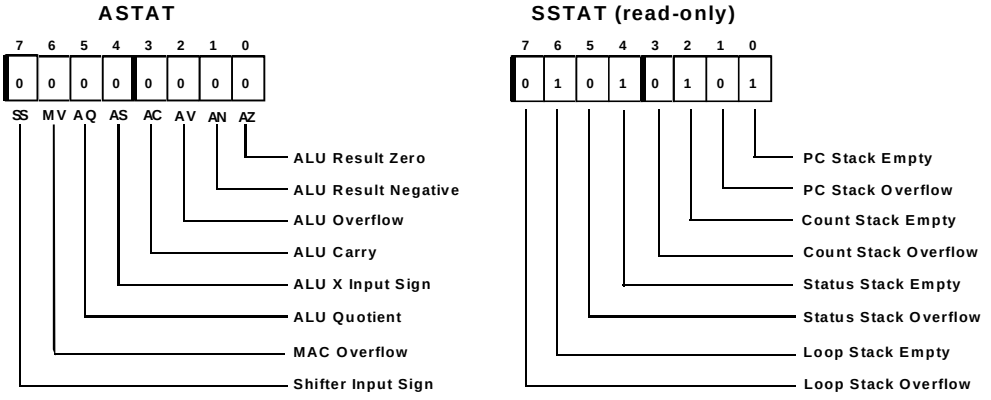


Figure B-23. ASTAT and SSTAT Registers

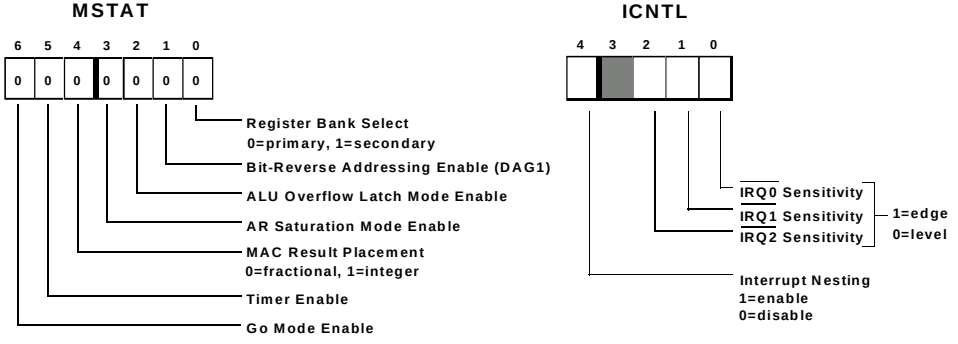


Figure B-24. MSTAT and ICNTL Registers

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These reserved bits must be set to zero.

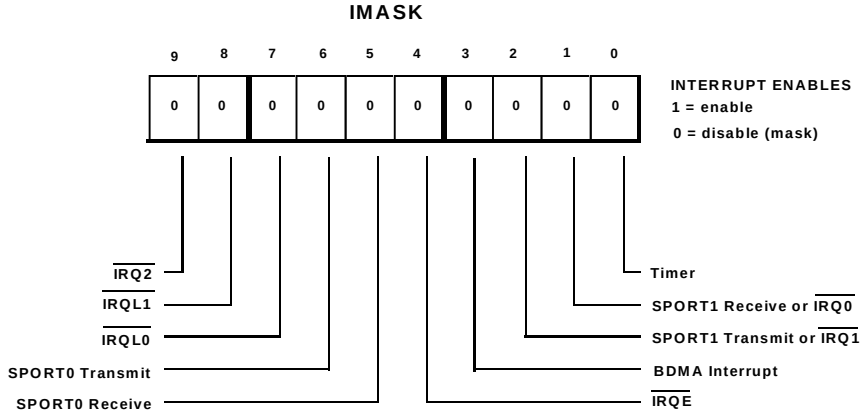


Figure B-25. IMASK Register

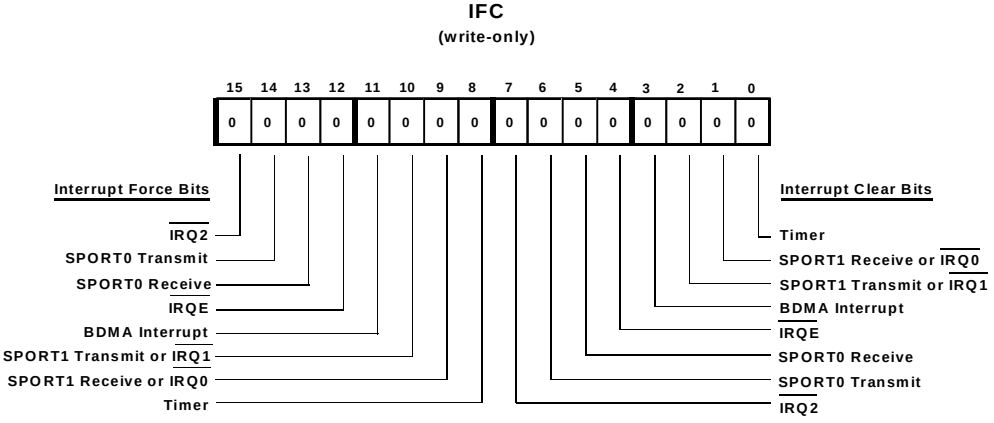


Figure B-26. IFC Register

Default bit values at reset are shown. If no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These reserved bits must be set to zero.