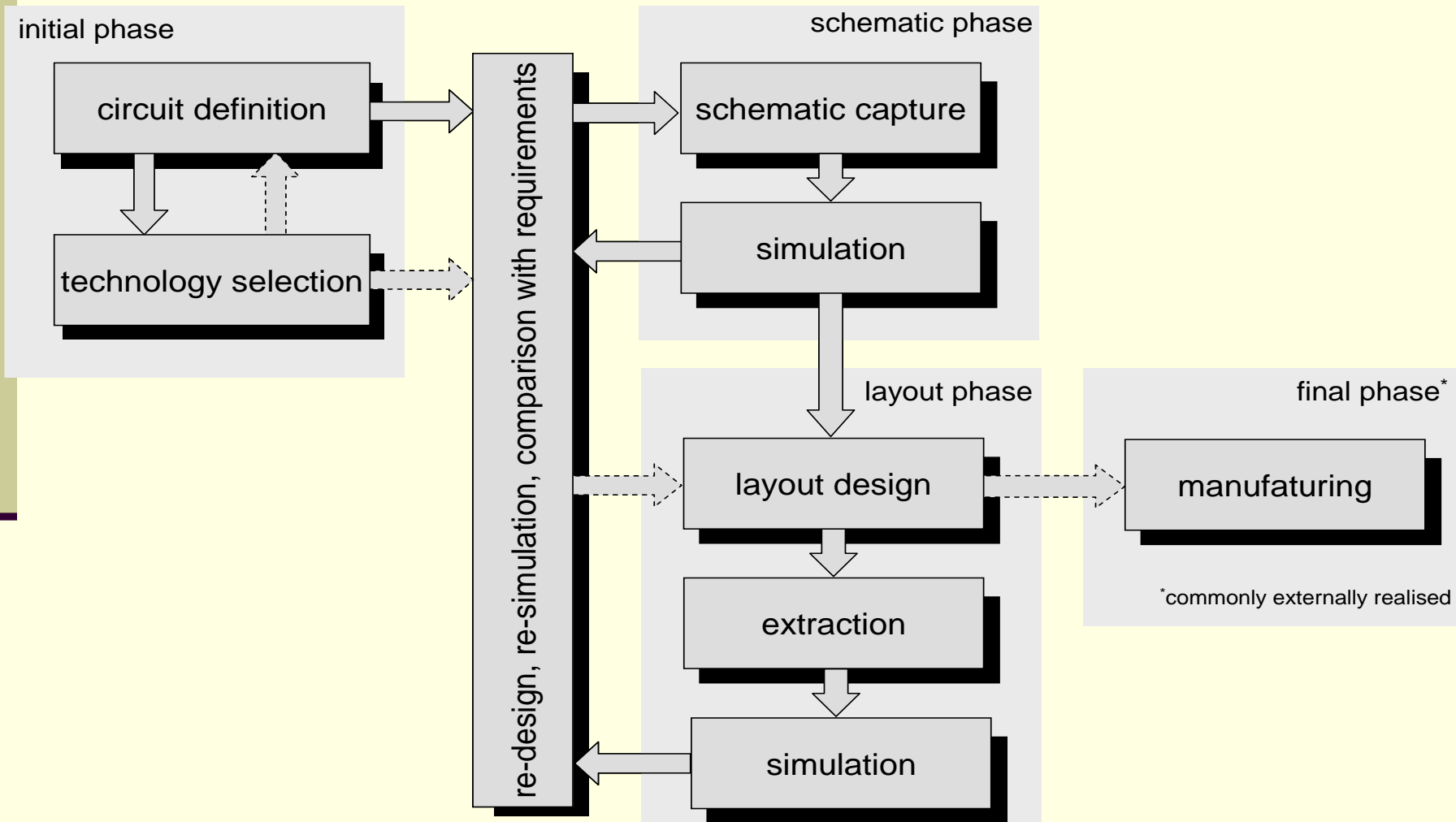


Návrhové prostredia v MG

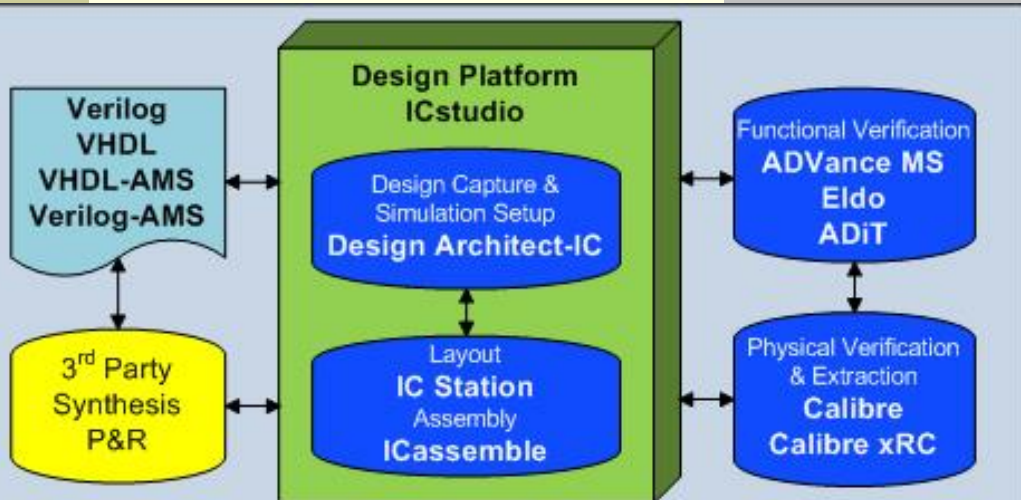
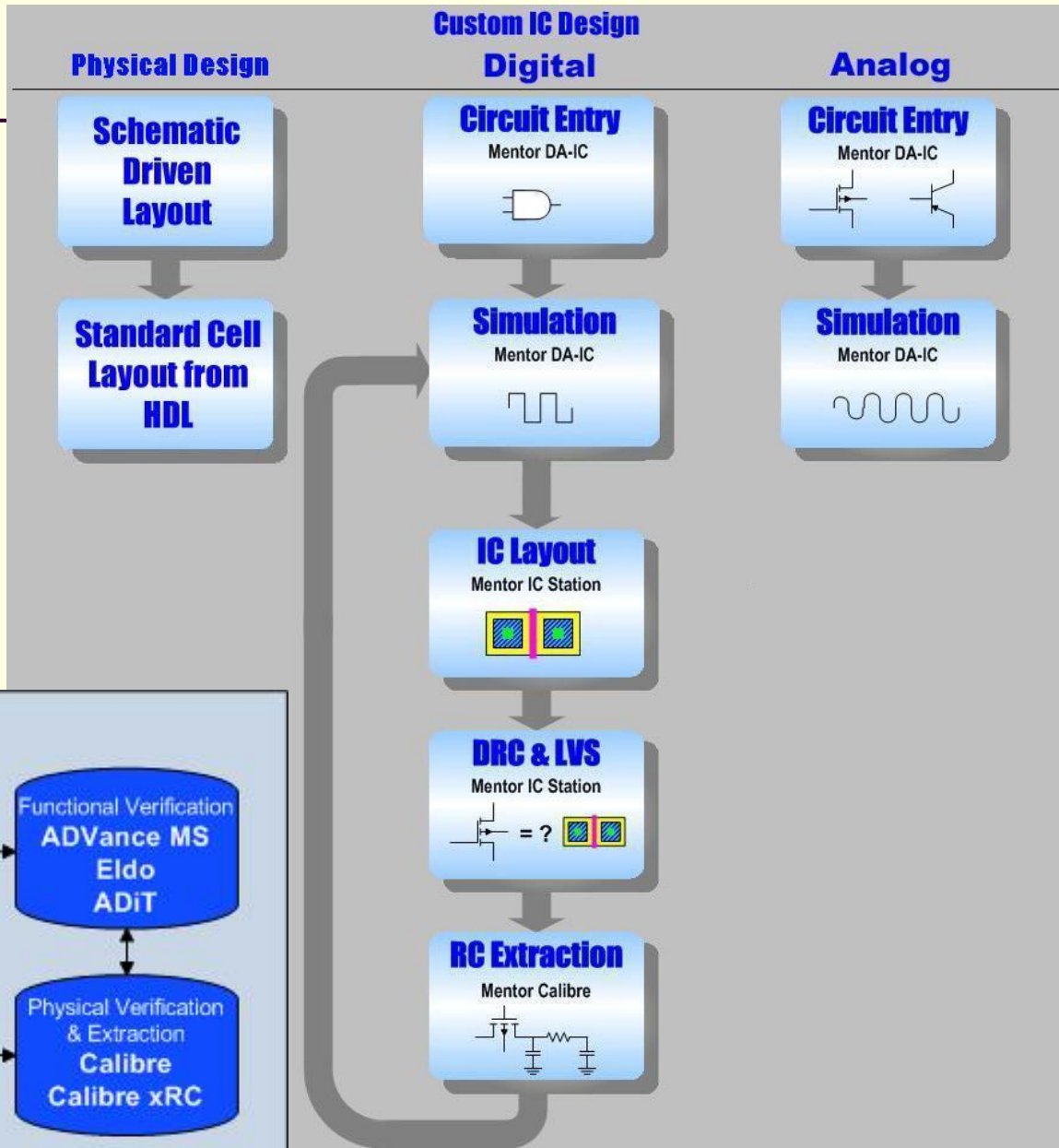
Pavol Galajda, KEMT, FEI, TUKE

Pavol.Galajda@tuke.sk

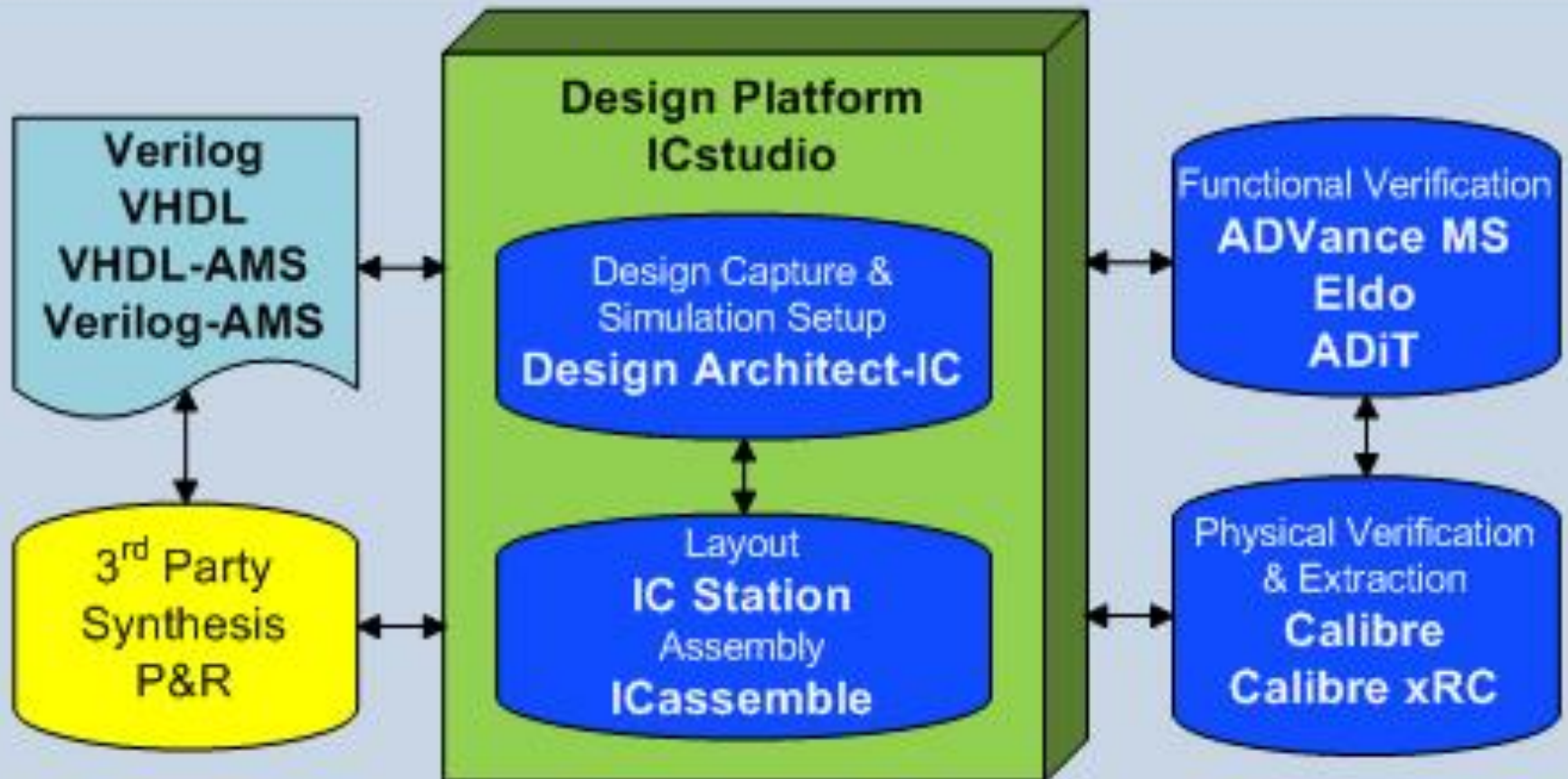
IC- postup pri návrhu



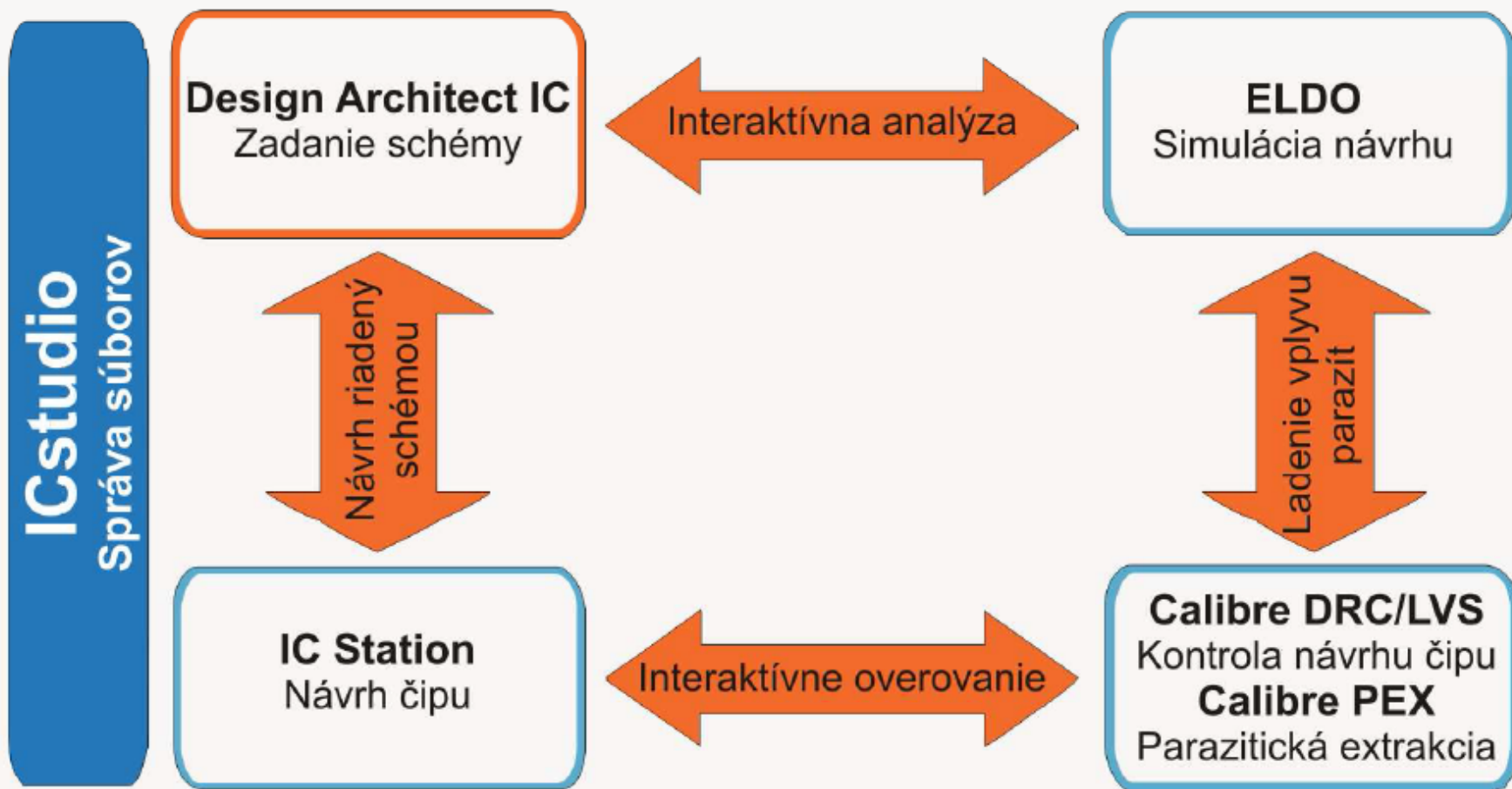
Postup pri návrhu prostredníctvom Mentor-Graphics



Postup pri návrhu prostredníctvom Mentor-Graphics



Kompletné riešenie návrhu IO od zadania schémy až po fyzický dizajn a overovanie obvodu

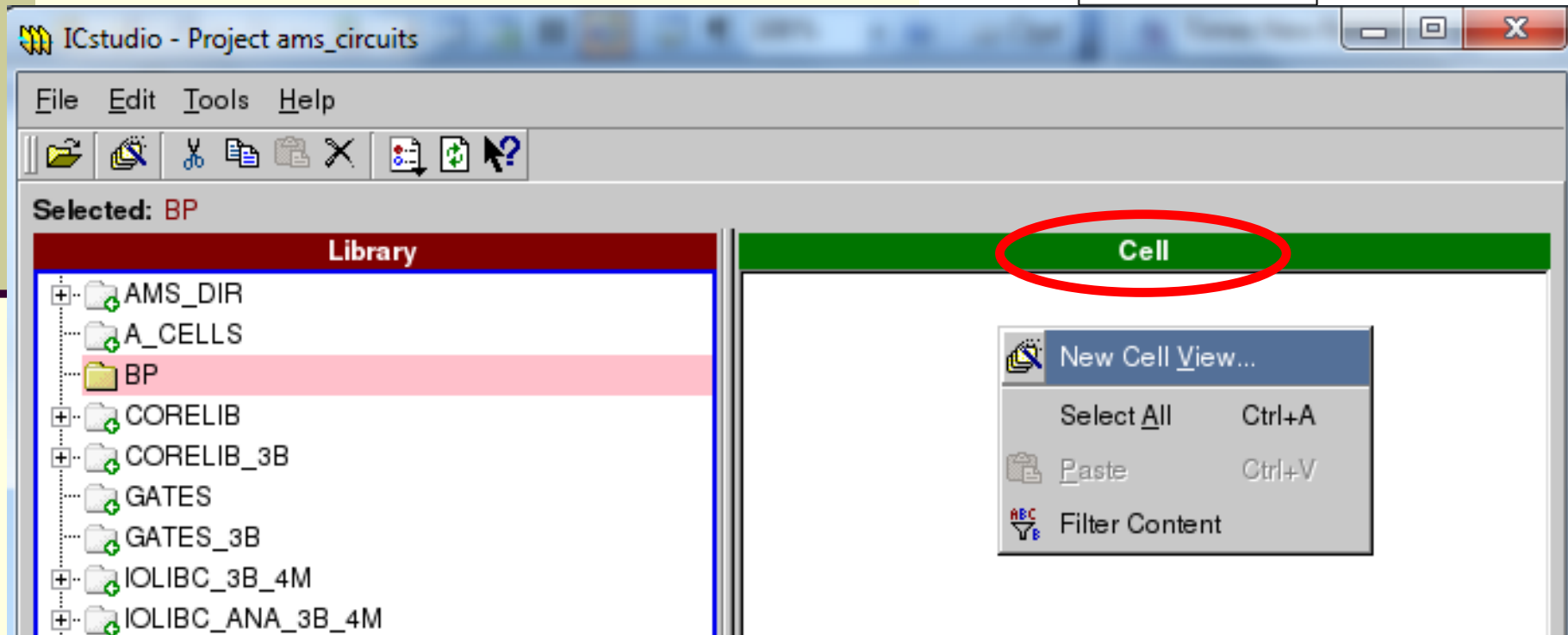
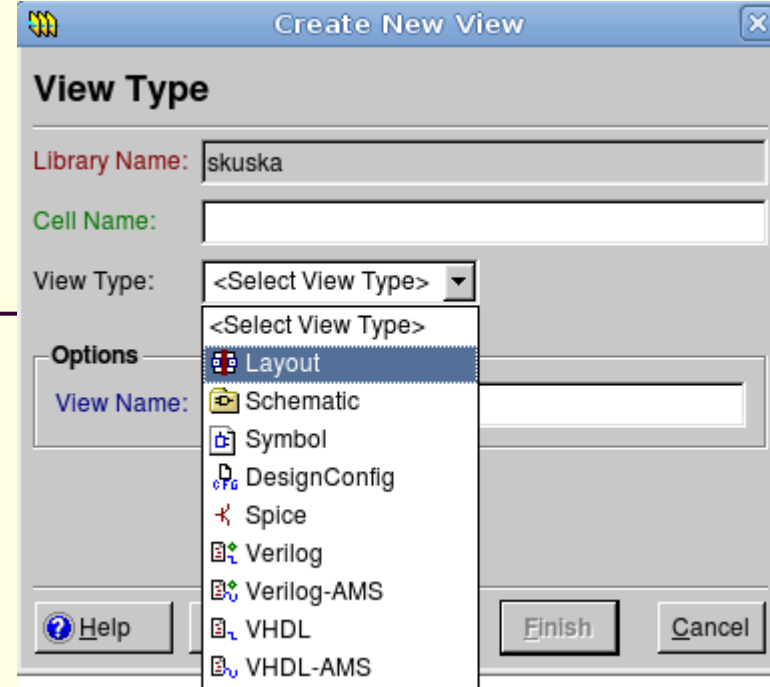


Vytvorenie projektu

The image shows a screenshot of the ICStudio software interface. The main window is titled "ICStudio - Project tukeic". The left sidebar displays a tree view of libraries, with "Mrkvicka" highlighted by a red circle. The right sidebar shows a "Library" pane with "AMS_DIR" and "A_CELLS" listed. A "New Library..." dialog box is open over the project window, indicating the process of creating a new library. The bottom status bar shows a log of messages, including "Note: Opening project "/home/palo/tukeic.proj"" and "Note: ICStudio startup complete".

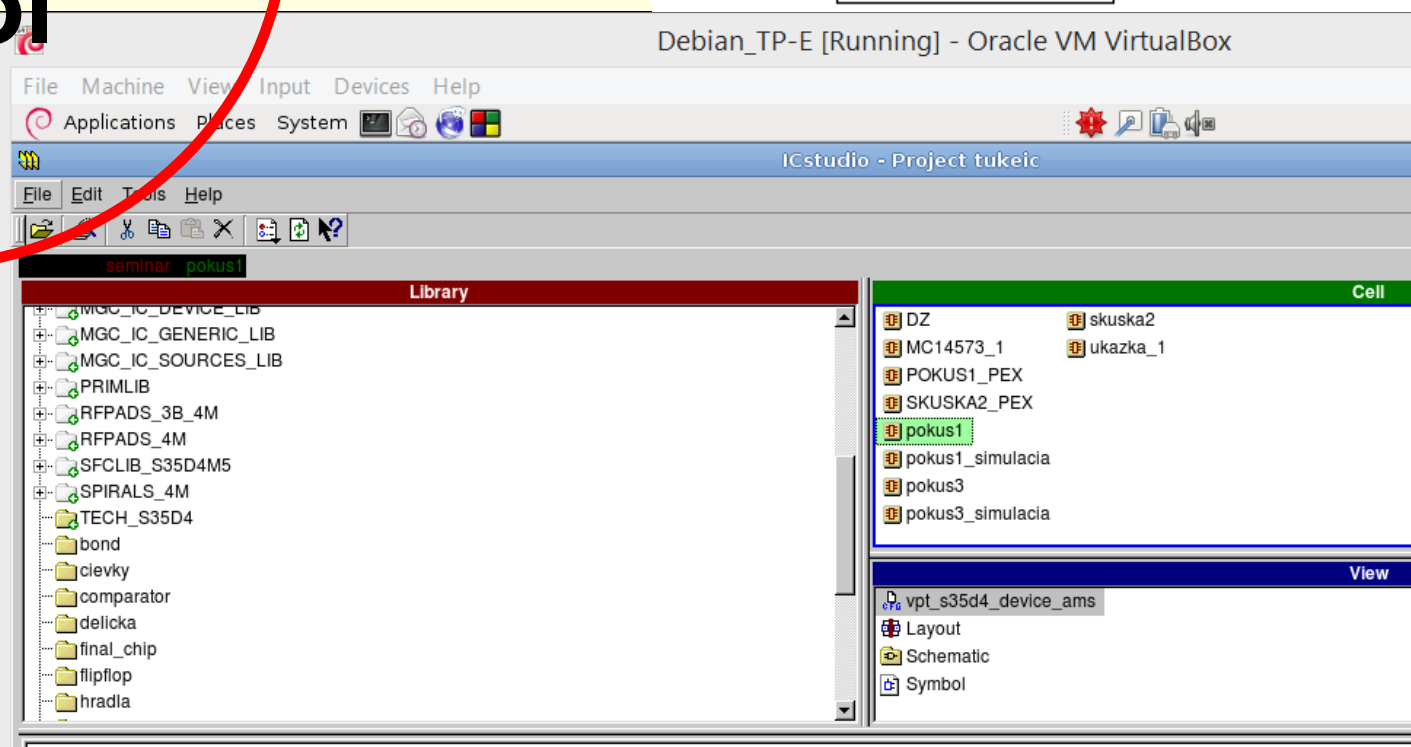
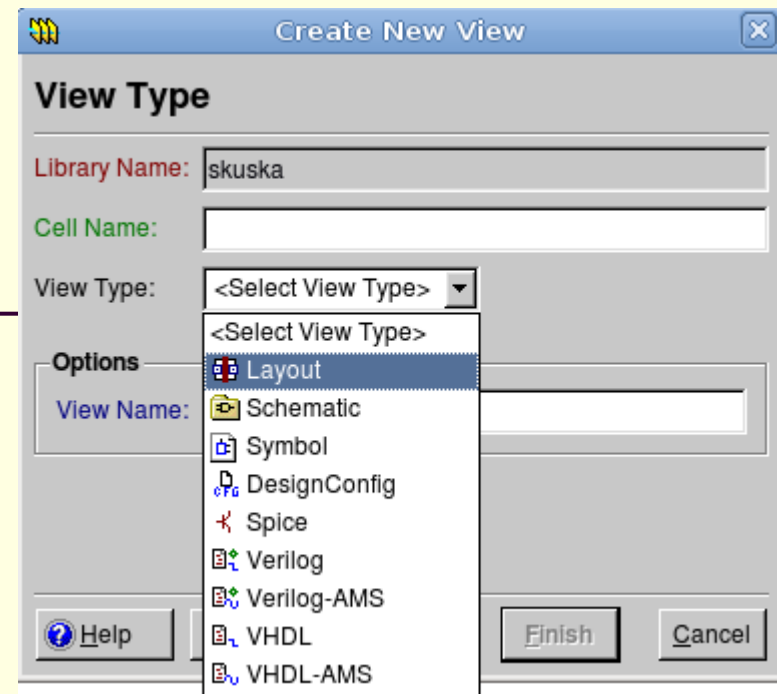
**V okne Create New Library
zvolíme názov našej knižnice,
!!!!!!!!!!!!!!!!!!!!
Priezvisko
!!!!!!!!!!!!!!!!!!!!**

Vytvorenie bunky



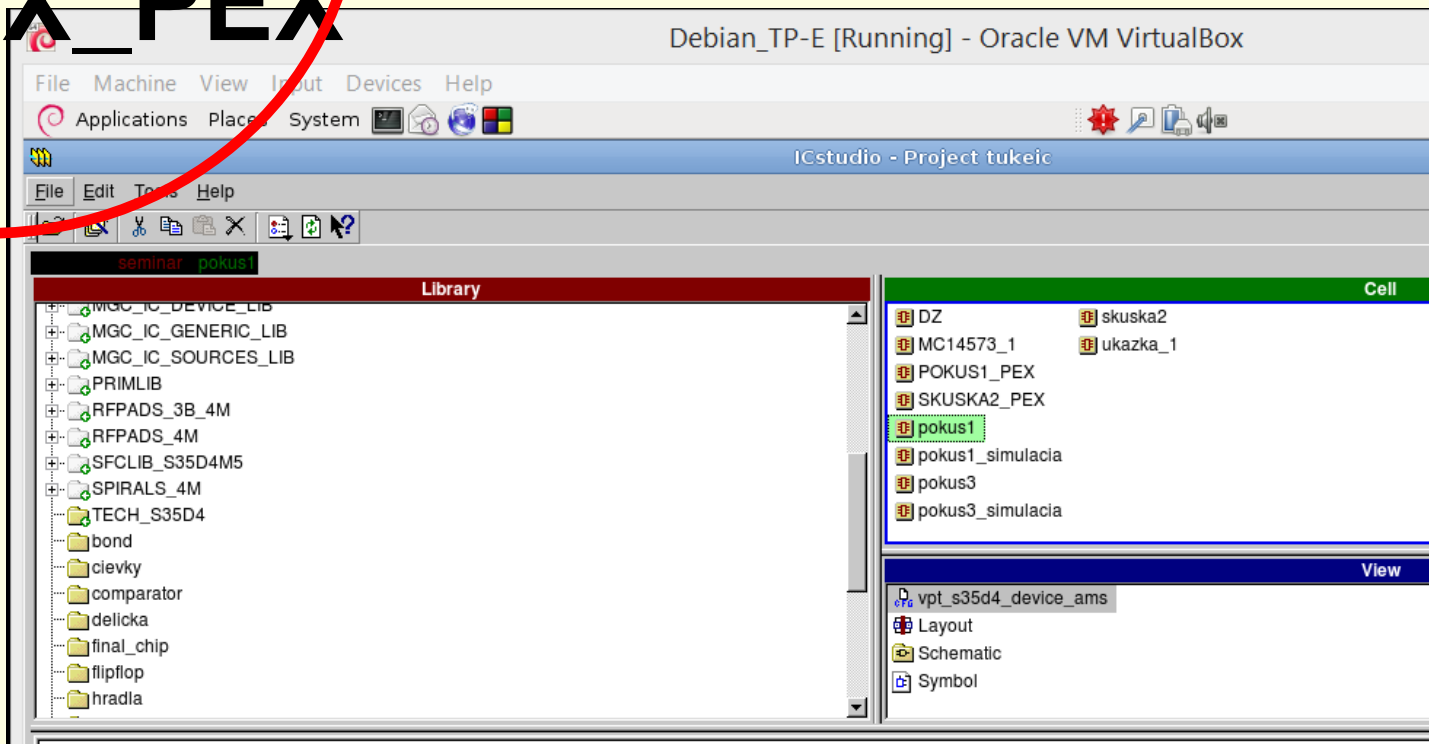
Vytvorenie bunky:

Schematic
Layout
Symbol
Spice



Vytvorenie bunky:

PokusX
PokusX_sim
PokusX_PEX



Kreslenie schém

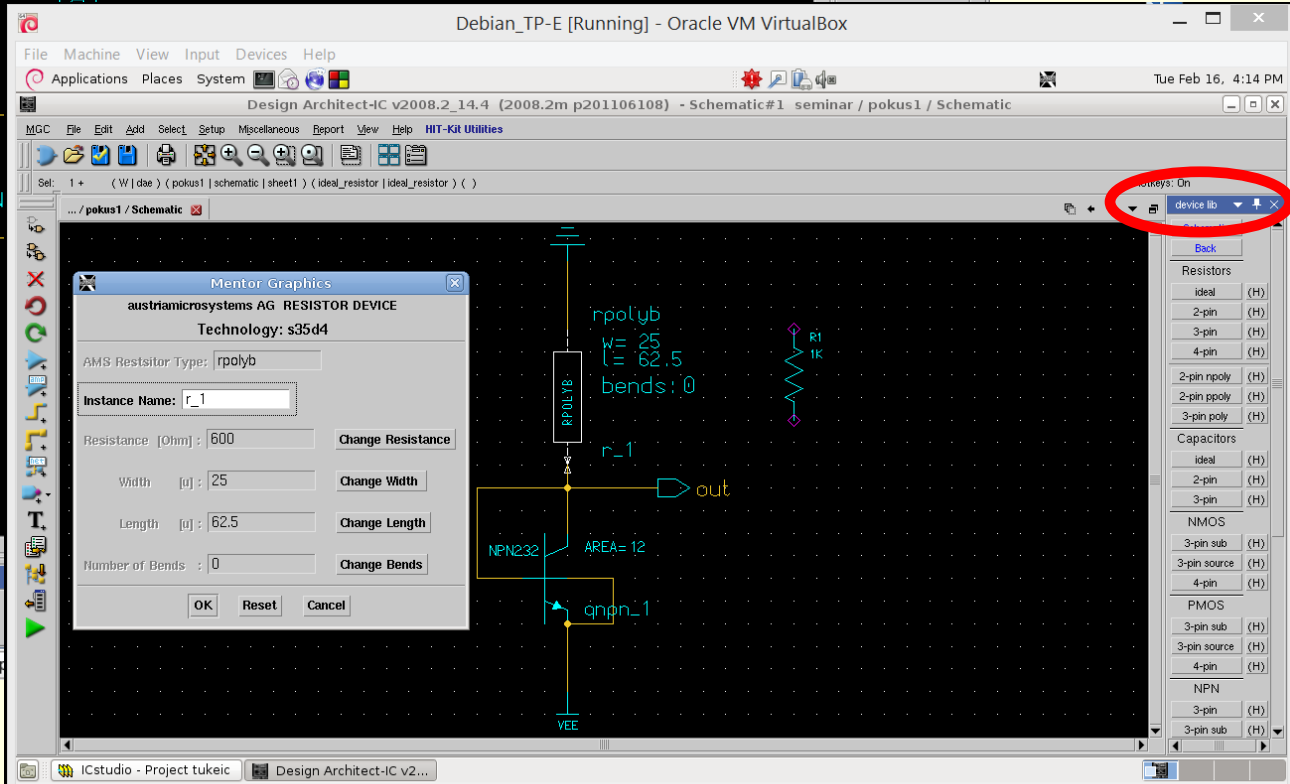
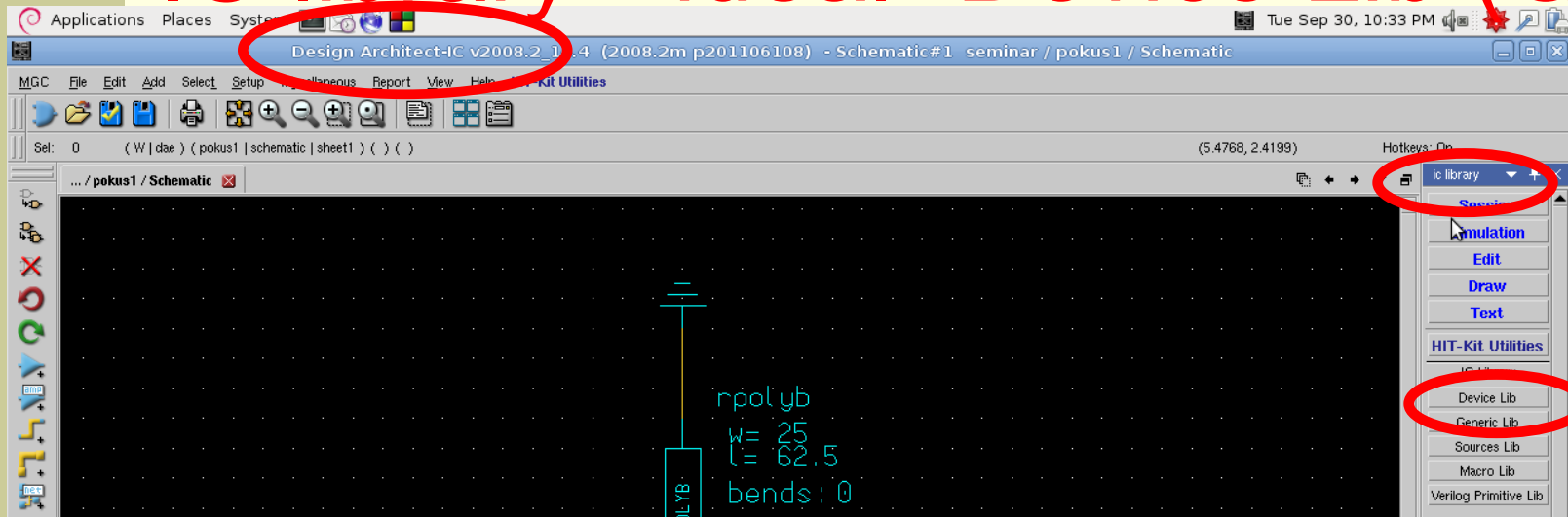
The image shows a screenshot of the ICStudio software interface. The main window is titled "ICStudio - Project tukeic". The interface is divided into several sections:

- Library:** A tree view on the left side containing various component libraries such as IOLIBV5_4M, IOLIB_3B_4M, IOLIB_4M, IOLIB_ANA_3B_4M, IOLIB_ANA_4M, Ivanov, MGC_IC_DEVICE_LIB, MGC_IC_GENERIC_LIB, MGC_IC_SOURCES_LIB, PRIMLIB, RFPADS_3B_4M, RFPADS_4M, SFCLIB_S35D4M5, SPIRALS_4M, TECH_S35D4, bond, cievky, comparator, culen_NPE, delicka, final_chip, flipflop, hradla, martinove_cipy, mixer, mixers_chip_full, npe, padlayout, pieskovisko, prevodnik, seminar, skuska, zosilnovac, zosilnovac_LNA, and zosilnovac_LNA_MZ.
- Schematic Editor:** The central workspace shows a schematic diagram on a black background. It includes a component labeled "PPOLYB" with properties: $w = 25$, $l = 62.5$, and $bends: 0$. Below it is a component labeled "NPN232" with $AREA = 12$ and a sub-component labeled "qnpn_1". The circuit is connected to a power supply (VCC) and ground (VEE). An output terminal is labeled "out".
- Terminal:** At the bottom of the window, there is a terminal window with the following text:

```
$$close_window(@discard, void, @false);  
$set_active_window("session");  
$set_active_window("session");  
$$close_session(void);
```
- Taskbar:** The Windows taskbar at the bottom shows several open applications, including "Downloads - File Brow...", "[mc [palo@KaktusDe...", "[TUKE - TUKE - Icewe...", "ICStudio - Project tukeic", and "Design Architect-IC v2...".

Red circles highlight the "Design Architect-IC v2008.2 14.4" window title bar and the "Schematic" tab in the taskbar.

IC library- "ideal" Device Lib (Q)



IC library- "ideal" Device Lib (Q)

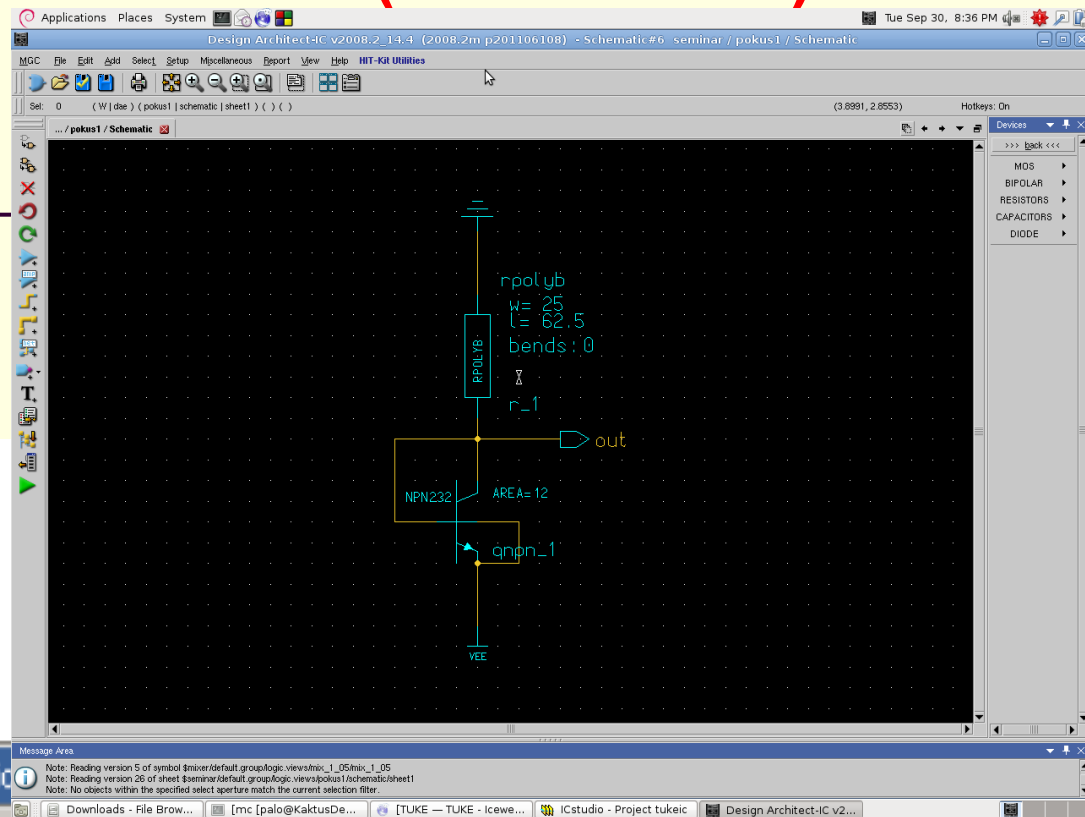
The image shows a screenshot of the Design Architect-IC v2008.2.14.4 software interface. The title bar indicates it is running in an Oracle VM VirtualBox environment on a Debian_TP-E system. The main window displays a schematic editor with a circuit diagram and a configuration dialog for an "austriamicrosystems AG RESISTOR DEVICE".

The configuration dialog, titled "Mentor Graphics austriamicrosystems AG RESISTOR DEVICE", is set to Technology: s35d4. The AMS Restsitor Type is "rpolyb". The Instance Name is "r_1". The Resistance is 600 Ohm, Width is 25 um, Length is 62.5 um, and Number of Bends is 0. The dialog includes buttons for "Change Resistance", "Change Width", "Change Length", "Change Bends", "OK", "Reset", and "Cancel".

The schematic diagram shows a circuit with a resistor labeled "r_1" connected to a power supply (VEE) and an output terminal "out". The resistor is labeled "RPOLYB" and has handwritten annotations: "w= 25", "l= 62.5", and "bends: 0". A transistor labeled "NPN232" is also present, with "AREA= 12" and "qnpn_1" annotations. A legend on the right shows a resistor symbol labeled "R1" with a "1K" value.

The software interface includes a menu bar (File, Machine, View, Input, Devices, Help), a toolbar, and a right-hand panel with a "device lib" dropdown menu and a list of components (Resistors, Capacitors, NMOS, PMOS, NPN). The system tray at the bottom shows "ICstudio - Project tukeic" and "Design Architect-IC v2...".

HIT-Kit Utilities- AMS (ALT+F6)



ic library

- Session
- Simulation
- Edit
- Draw
- Text
- Library**
- Simulation
- Edit
- Draw
- Text
- HIT-Kit Utilities**
- IC Library
- Device Lib
- Generic Lib
- Sources Lib
- Macro Lib
- Verilog Primitive Lib

1.

2.

Device

- >>> back <<<
- MOS
- BIPOLAR**
- RESISTORS
- CAPACITORS
- DIODE
- BIPOLAR
- npn**
- pnplat2
- pnpvert10

3.

4.

Mentor Graphics

austrimicrosystems AG BIPOLAR TRANSISTOR DEVICE

Technology: s35d4

Instance Name: **qnpn_1**

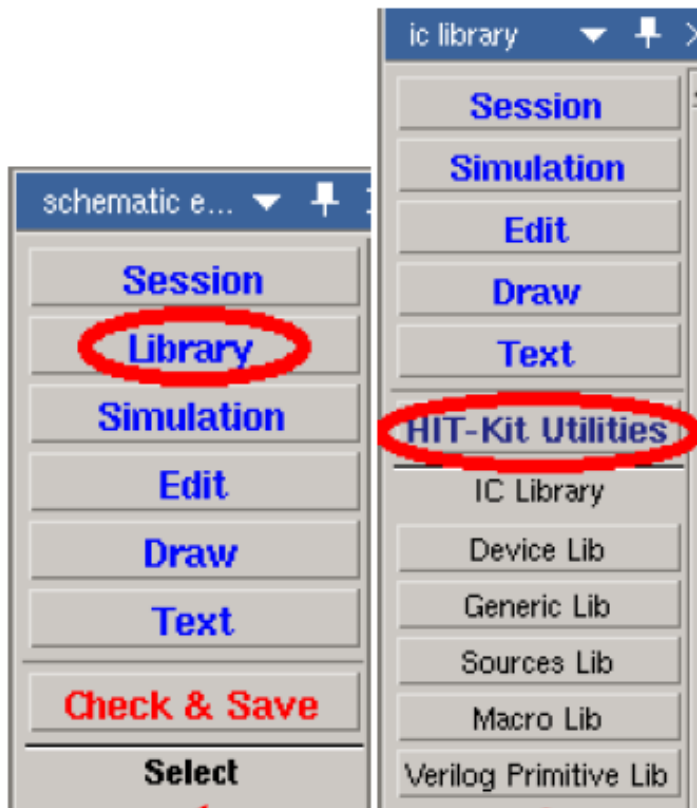
Transistor Type: npn232 **Change Type**

Emitter Area [u^2]: 12 **Change Area**

OK Reset Cancel

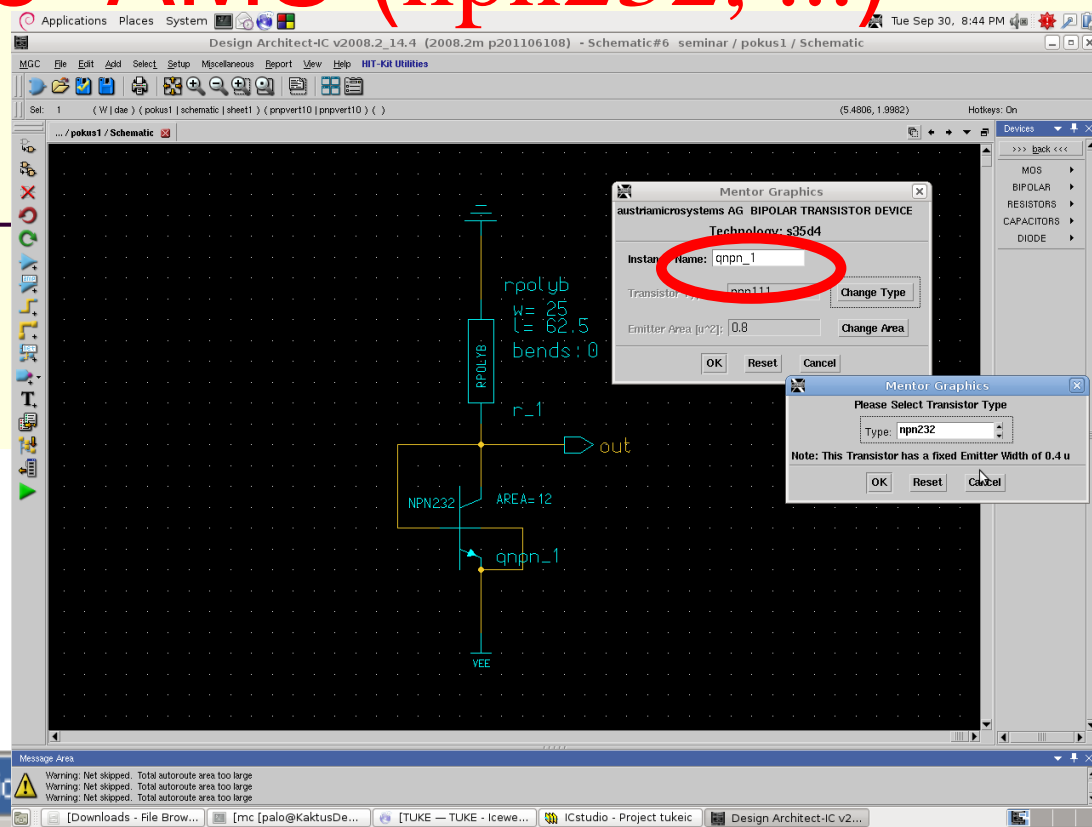
5.

HIT-Kit Utilities- AMS (nnp232, ...)



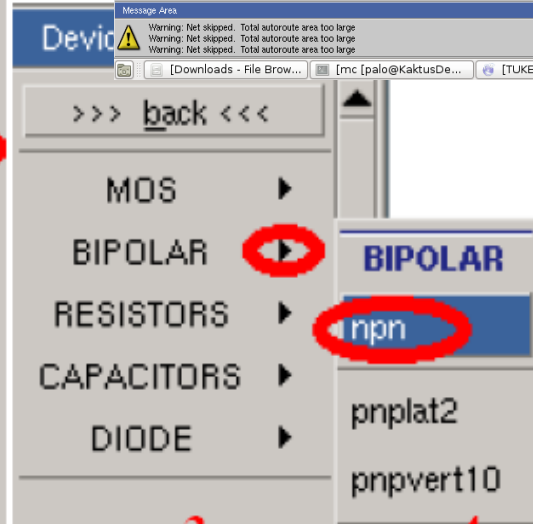
1.

2.



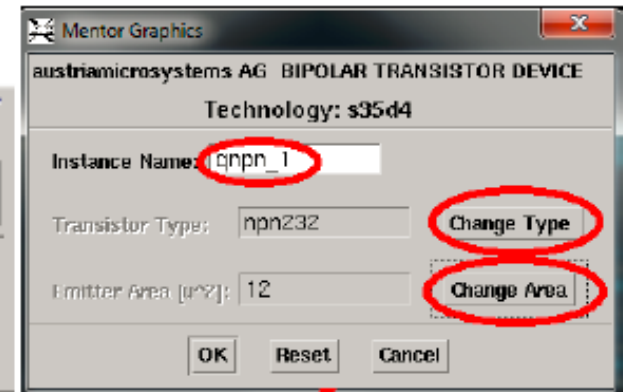
3.

4.



3.

4.



5.

HIT-Kit Utilities- AMS (ALT+F6)

The image shows a screenshot of a CAD environment, likely a virtual machine running Debian TP-E. The main window is titled "Design Architect-IC v2008.2_14.4 (2008.2.m p201106108) - Schematic#1 seminar / pokus1 / Schematic". The interface includes a menu bar (File, Machine, View, Input, Devices, Help), a toolbar, and a panel on the right showing a component library. The library is currently displaying "Resistors" and "Capacitors". A red circle highlights the "device lib" dropdown menu in the top right corner.

A dialog box titled "Mentor Graphics" is open, showing the configuration for an "austriamicrosystems AG BIPOLAR TRANSISTOR DEVICE" with Technology: s35d4. The Instance Name is "qnpn_1". The Transistor Type is "npn232" and the Emitter Area is "12". The dialog box has "OK", "Reset", and "Cancel" buttons.

The schematic editor shows a circuit diagram with a transistor model labeled "NPN232" and "AREA=12". The transistor is connected to a resistor labeled "R1" and a capacitor labeled "C1". The output of the circuit is labeled "out". Handwritten notes in cyan text are visible: "rpolyb", "w= 25", "l= 62.5", and "bends: 0".

The bottom left corner of the window shows a text area with the following content:

```
// Design Architect-IC v2008.2_14.4 (2008.2.m p201106108) - Schematic#1 seminar / pokus1 / Schematic
// EDDM-IC v2008.2_14.2
// Core Libraries v2008.2
//
// Copyright Me
//
// All
//
// THIS WORK CONTAINS TRADE SECRETS AND IS THE PROPERTY OF
// MENTOR GRAPHICS CORPORATION. ALL RIGHTS RESERVED. NO PART
// OF THIS WORK MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM
// OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING
// PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE
// AND RETRIEVAL SYSTEM, WITHOUT PERMISSION IN WRITING FROM
// MENTOR GRAPHICS CORPORATION.
```

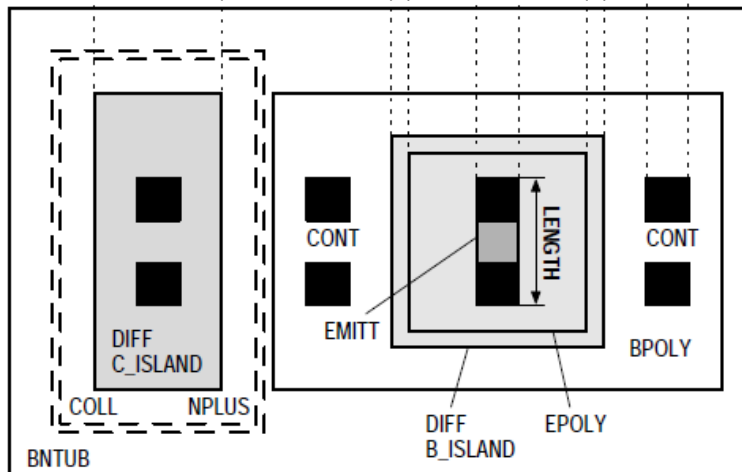
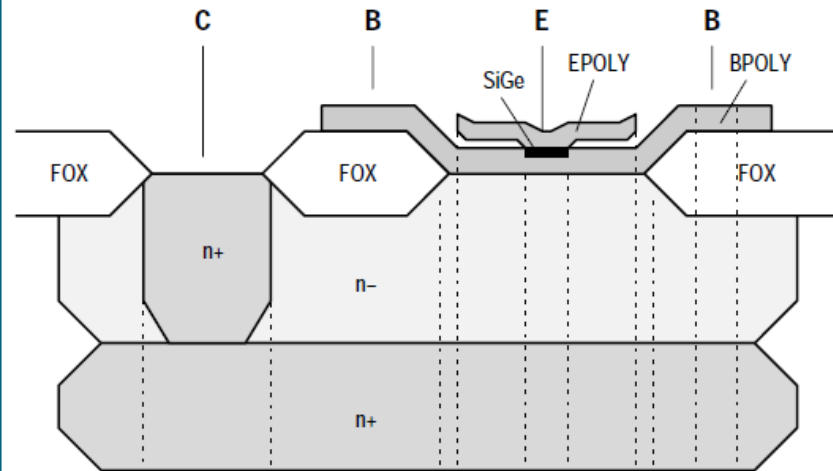

HIT-Kit Utilities- AMS

High Speed HBT

5.3.2 NPN121

Note: EMITTER LENGTH can be changed.

All BASE stripes must be connected to a single terminal.



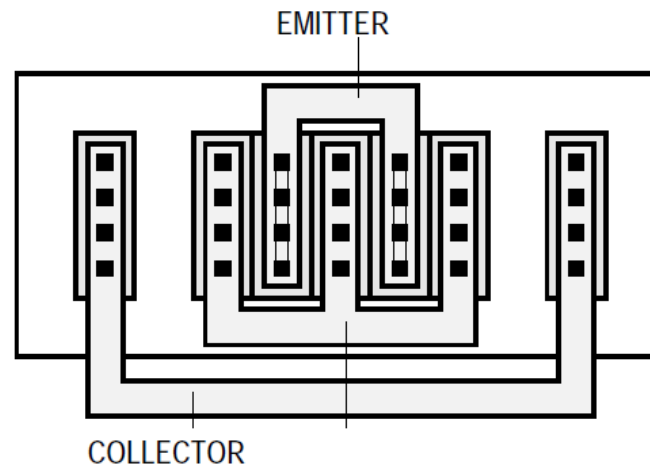
5.3.5 NPN232

Note: EMITTER LENGTH can be changed.

All COLLECTOR stripes must be connected to a single terminal.

All BASE stripes must be connected to a single terminal.

All EMITTER stripes must be connected to a single terminal.



5.3.1 NPN111 ...

5.3.2 NPN121 ...

5.3.3 NPN132 ...

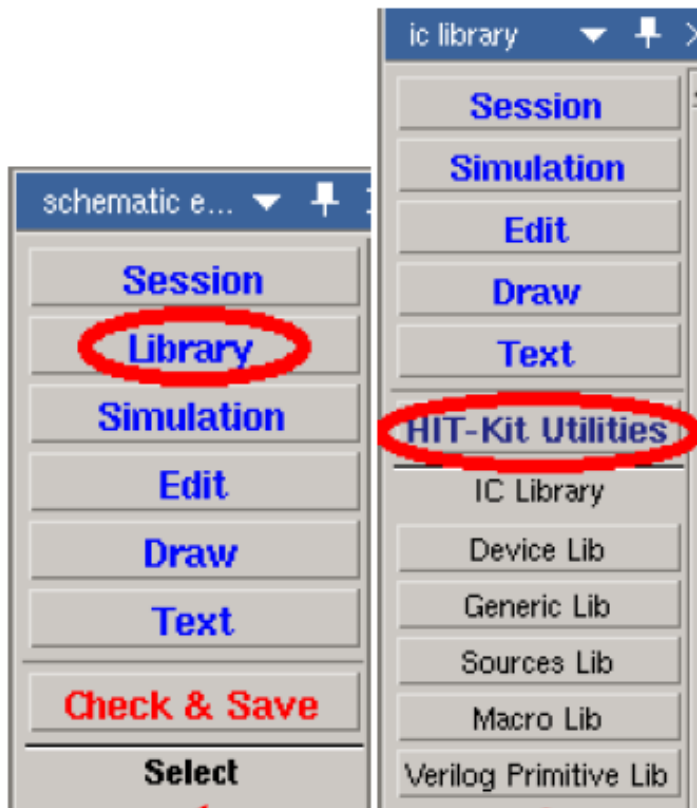
5.3.4 NPN143 ...

5.3.5 NPN232 ...

5.3.6 NPN243 ...

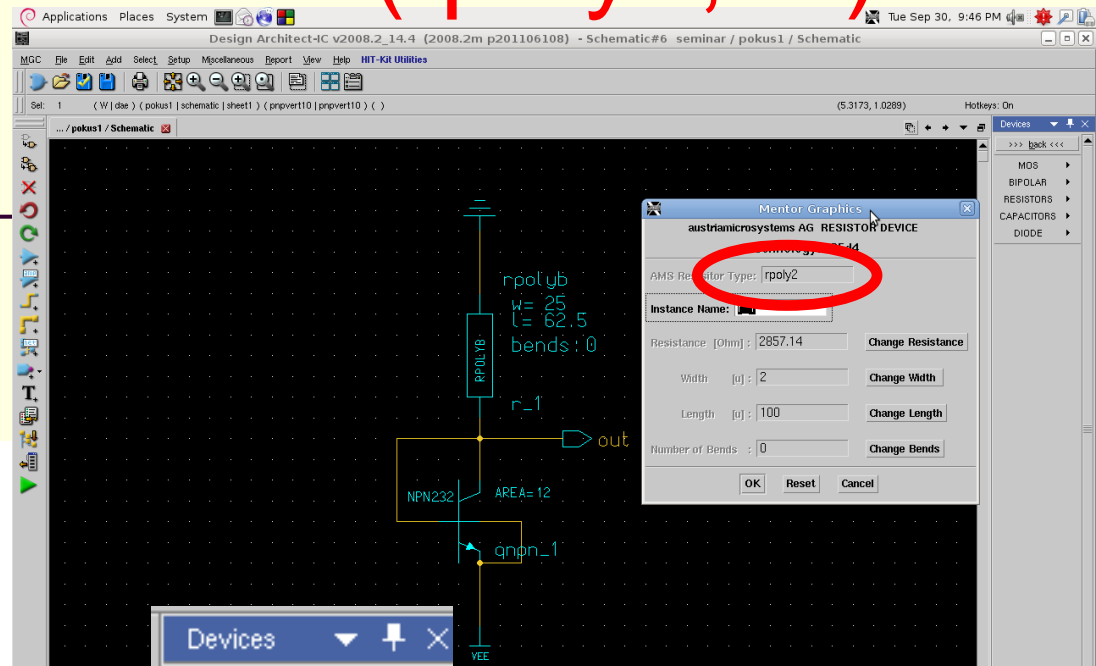
5.3.7 NPN254 ...

HIT-Kit Utilities- AMS (rpoly2, ...)

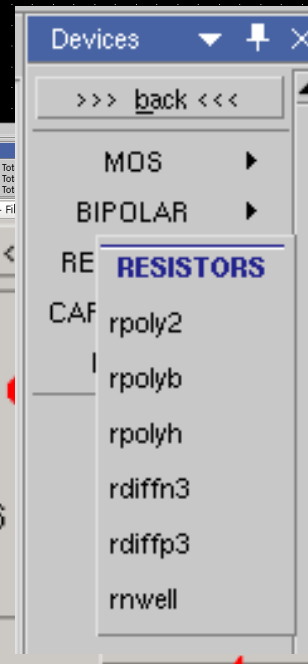


1.

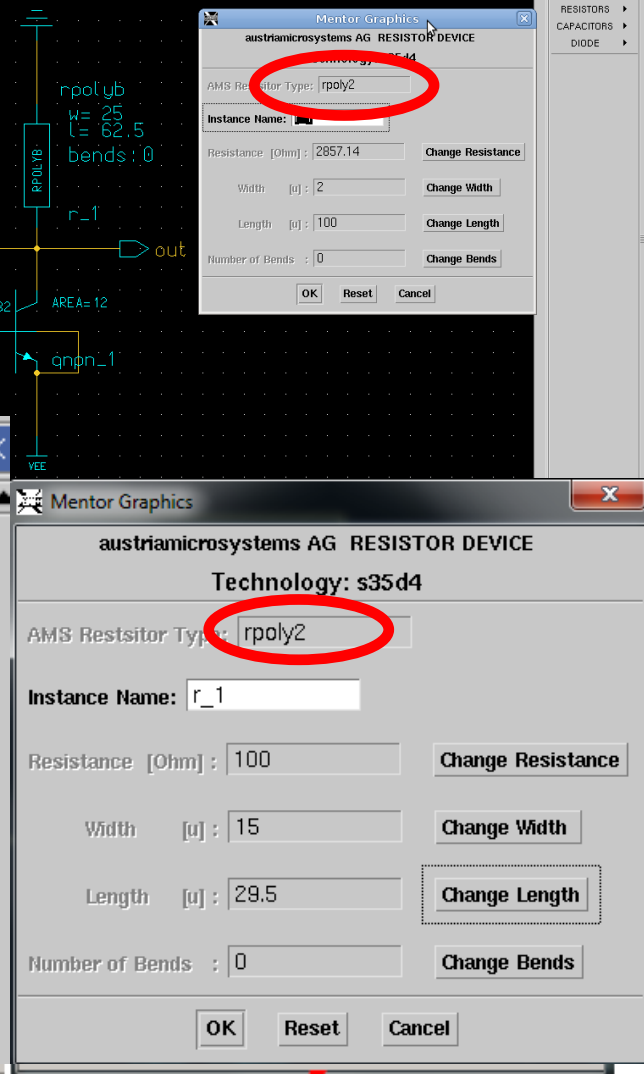
2.



3.

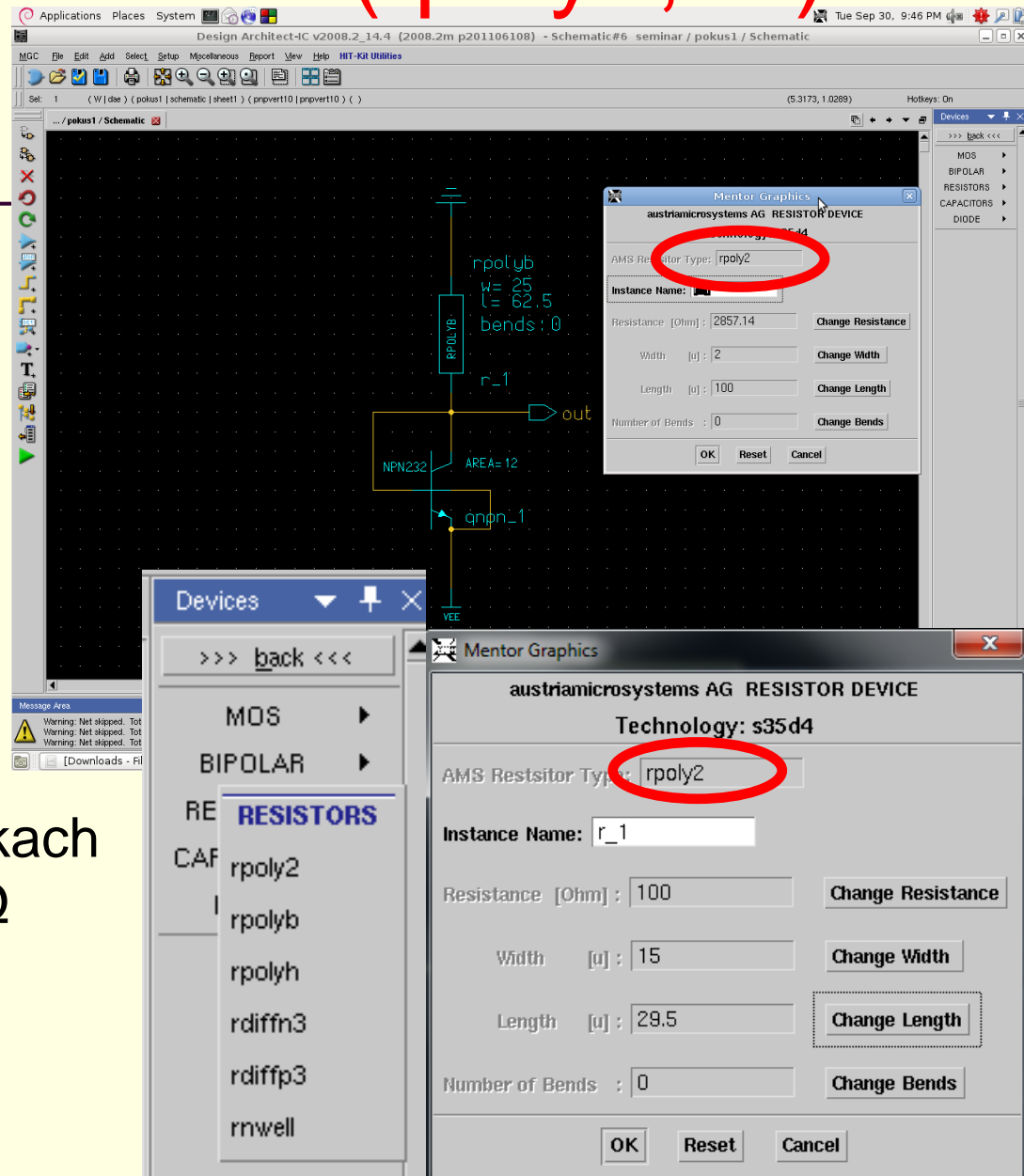


4.



5.

HIT-Kit Utilities- AMS (rpoly2, ...)



Hodnoty odporu v desiatkach
až niekoľkých stovkách Ω
Rpoly2

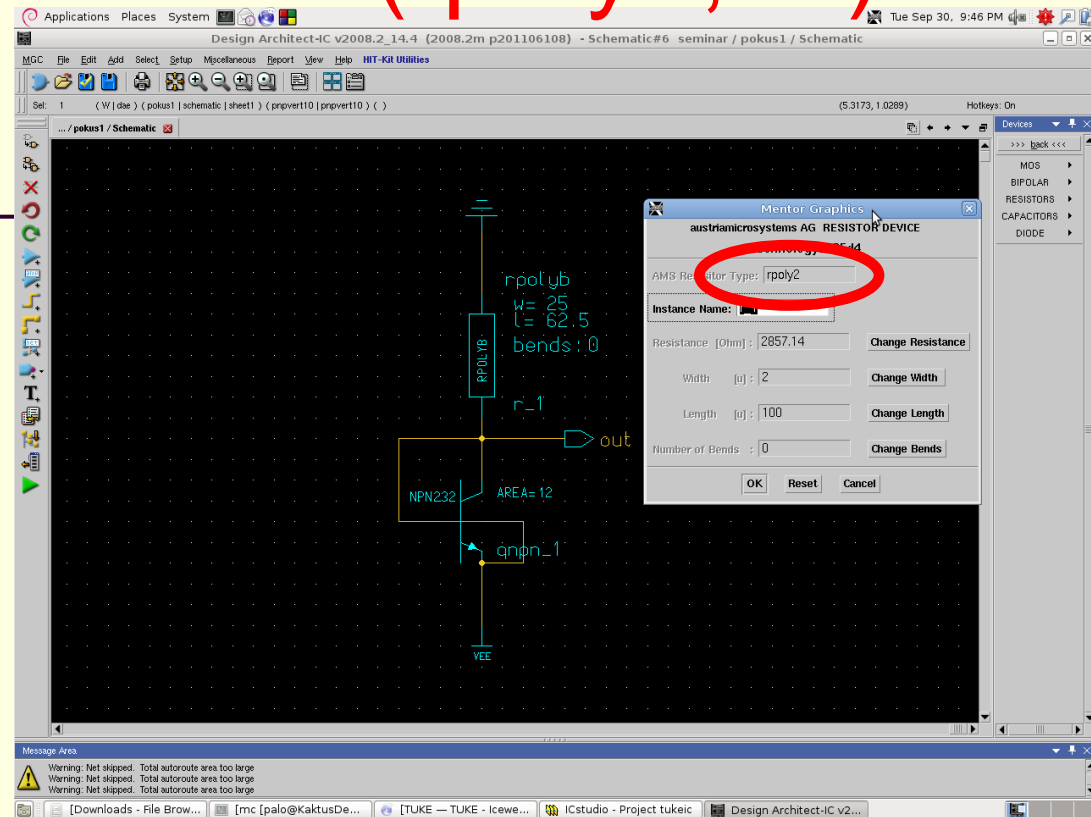
Pre vyššie hodnoty
Rpolyb a **Rpolyh**

HIT-Kit Utilities- AMS (rpoly2, ...)

Dĺžka rezistora je úmerná jeho odporu, pričom je potrebné podľa rezistivity a dovolenej prúdovej hustoty odporovej vrstvy zvoliť vhodný typ rezistora pre danú hodnotu a prúd tak, aby mal **prípustné rozmery**.

Väčšinu plochy čipu zaberajú rezistory, ktorých šírka musí rovnako ako šírka vodivých spojov s dostatočnou rezervou **zodpovedať maximálnej prúdovej hustote danej vrstvy** určenej výrobcom.

Niekedy je vhodné rezistor rozdeliť na dva paralelné rezistory dvojnásobného odporu, pretože výrobca neodporúča rozmery rezistorov, kde šírka je väčšia ako dĺžka.



HIT-Kit Utilities- AMS (cmim)

The screenshot shows the Design Architect-IC v2008.2_14.4 interface. The main window displays a schematic diagram with components: a top rail, a resistor labeled 'RPOLYB', a node labeled 'r_1', an NPN transistor labeled 'NPN232' with 'AREA=12', a node labeled 'qnpn_1', and a bottom rail labeled 'VEE'. An output terminal labeled 'out' is connected to the node between the resistor and the transistor. Handwritten blue annotations include 'rpolymb', 'w = 25', 'l = 62.5', and 'bends: 0'. A 'Devices' panel on the left lists MOS, BIPOLAR, RESISTORS, and CAPACITORS. The 'CAPACITORS' list includes 'cpolya', 'cvar', 'cmim', 'csink', and 'cstack'. A 'Mentor Graphics' dialog box is open, titled 'austriamicrosystems AG CAPACITOR DEVICE'. The 'Technology' field is set to 's35d4' and circled in red. The 'AMS Capacitor Type' is 'cmim'. The 'Instance Name' is 'c_1'. Parameters include 'Cap [pF]: 0.509', 'Area [u^2]: 400', and 'Peri [u]: 80'. 'Capacitor's Shape' is set to 'Rectangular' with 'Width [u]: 20' and 'Length [u]: 20'. Buttons for 'Change Capacitance', 'Change Area', 'Change Perimeter', 'Change Width', and 'Change Length' are present. The dialog has 'OK', 'Reset', and 'Cancel' buttons. A red '5.' is written in the bottom right corner of the dialog.

4.

no large
no large
no large

Kreslenie schém- F3= Add Wire

The image shows a screenshot of the Design Architect-IC v2008.2.14.4 software interface. The main window displays a schematic diagram on a black grid background. The diagram includes a vertical wire connected to a ground symbol at the top, labeled "RPOLYB". A yellow wire branches off from this vertical wire, leading to an output terminal labeled "out". Another yellow wire branches off from the same junction, leading to a component labeled "qnpn_1". A third yellow wire branches off from the junction, leading to a component labeled "NPN232". The component "NPN232" has the property "AREA=12" associated with it. The bottom terminal of the "qnpn_1" component is connected to a ground symbol labeled "VEE". Handwritten text in green and yellow on the schematic includes "rpolyb", "w= 25", "l= 62.5", "bends: 0", "r_1", and "qnpn_1".

The software interface includes a menu bar with "File", "Edit", "Tools", and "Help". A toolbar with various icons is located below the menu bar. The "Add" menu option is circled in red. The right side of the interface features a vertical toolbar with buttons for "Session", "Library", "Simulation", "Edit", "Draw", "Text", "Check & Save", "Select", "By Property", "Unselect All", "Edit", "Move", "Copy", "Delete", "Undo", "Flip", "Rotate", "Properties", "Add", "Instance", "Wire", "Bus/Bundle", "Add Source", "Property", and "Name". The bottom of the interface has a "Message Area" with the following text:

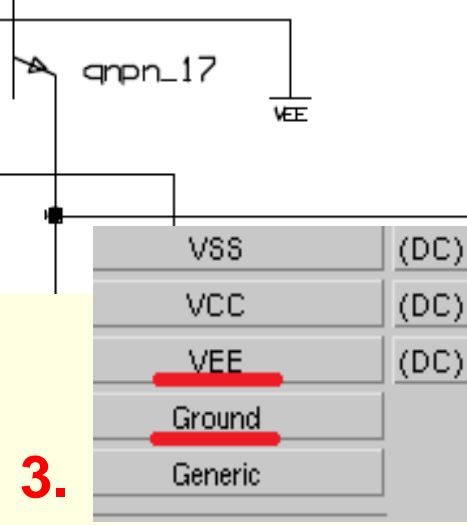
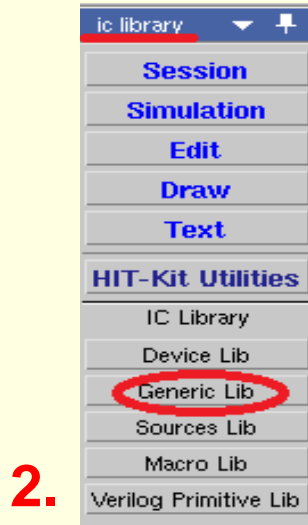
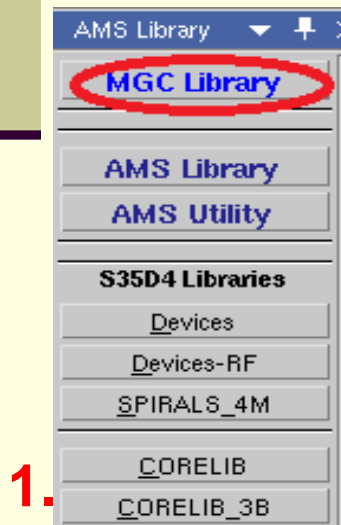
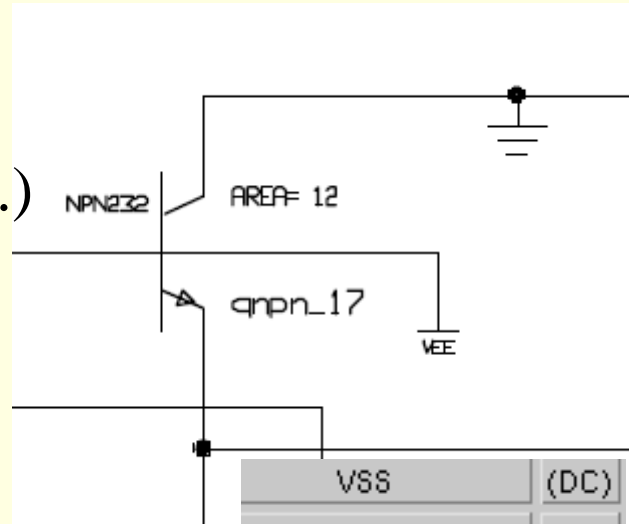
Note: Reading version 26 of sheet \$seminar/default.group.logic.views/pokus1/schematic/sheet1
Note: austriamicrosystems 'HIT-Kit Utilities' menu added
Note: HIT-Kit Version 3.70, Copyright (c) austriamicrosystems AG, 1991-2005

Porty

Port **VEE**, nájdeme v ponuke **Generic Library** → **VEE**.
Slúži ako odkaz pre ostatné porty **VEE**, aby bol návrh prehľadnejší.

Z **AMS Library** pomocou **MGC Library** spať do **IC library**,
kde je **Generic Library**.

Nájdeme tu aj „zem“ **Ground** = 0V (ref. pot.)



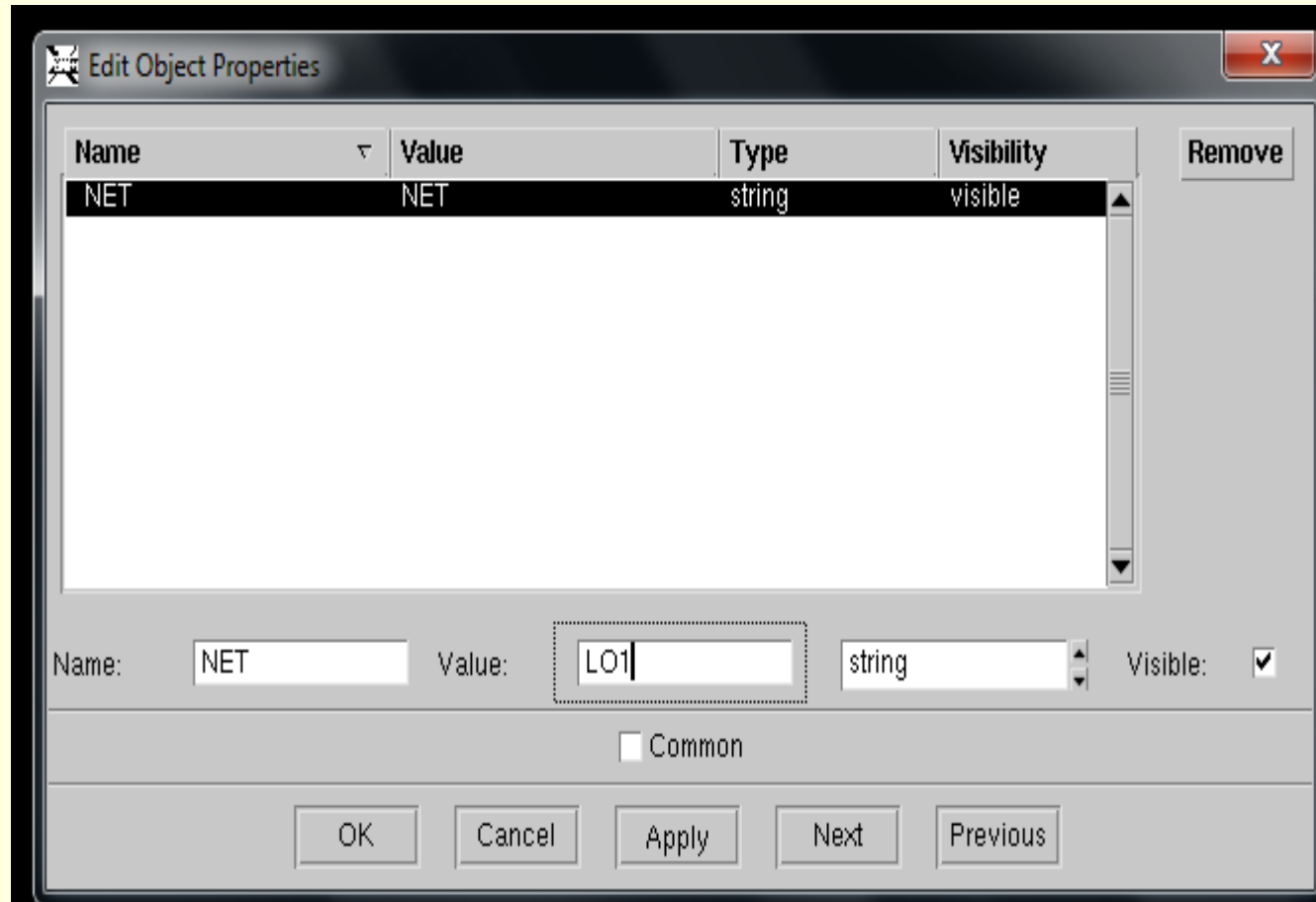
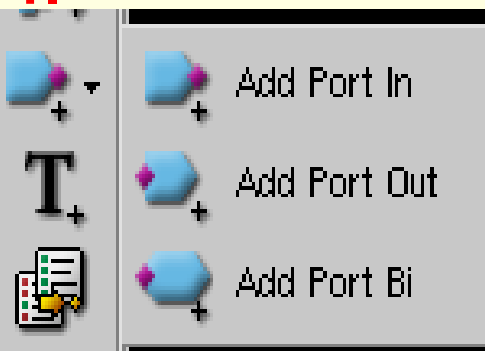
Porty- Vloženie portov

LO1 

2. - „Q“

Ľavá lišta

1.



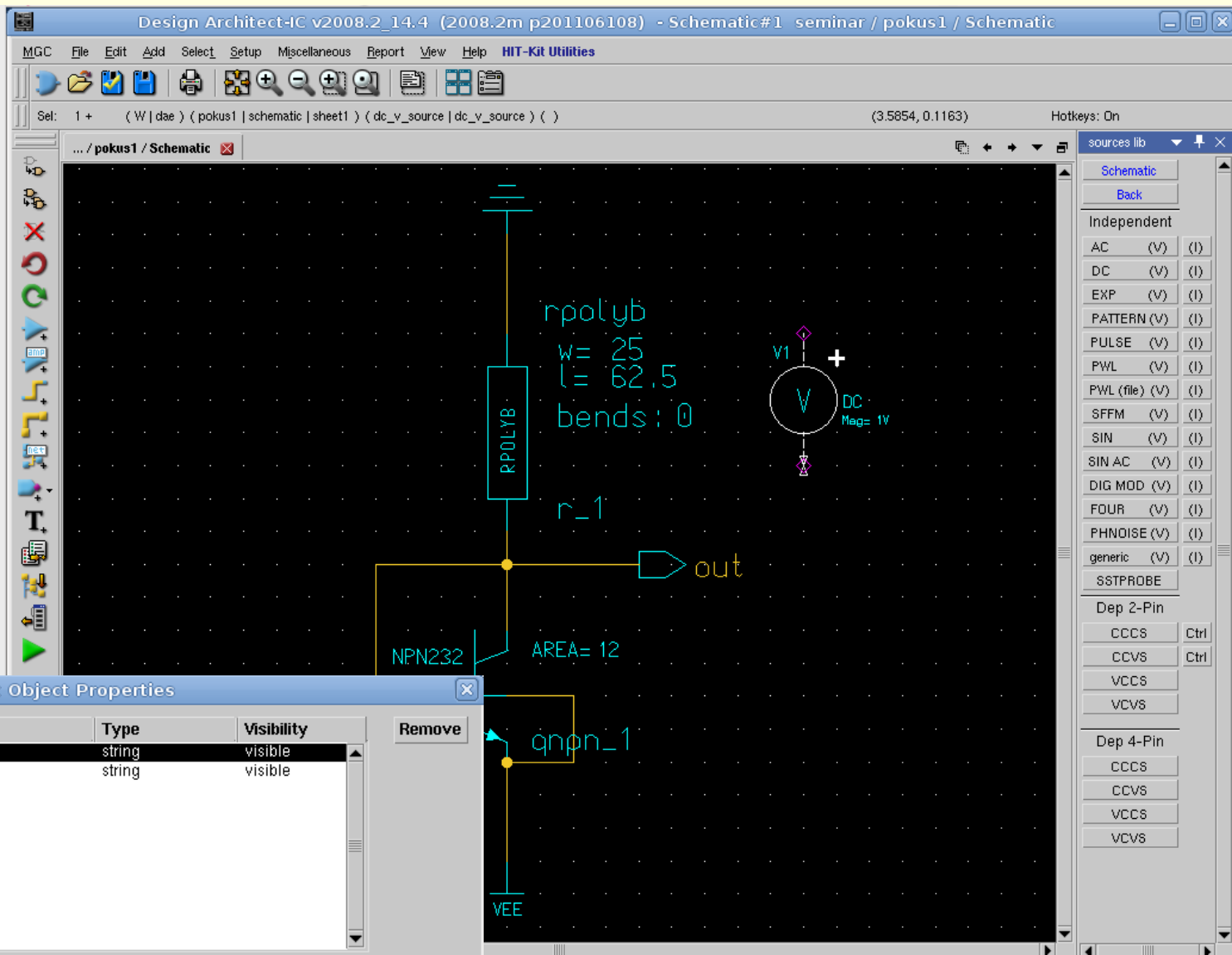
NET 

Zdroje V IC Library vyberieme Sources Library → DC (V)

1.

ic library

- Session
- Simulation
- Edit
- Draw
- Text
- HIT-Kit Utilities
- IC Library
- Device Lib
- Generic Lib
- Sources Lib
- Macro Lib



Edit Object Properties

Name	Value	Type	Visibility	Remove
DC	1V	string	visible	
INST	V1	string	visible	

Name: DC Value: 1V Type: string Visible:

Common

OK Cancel Apply Next Previous

2.-, "Q"- okno, definujúce parametre zdroja

Zdroje- Vloženie zdrojov

Add Fourier (Multi-tone) Source

Source Type:
 Voltage Current
DC Value (DC analysis only):

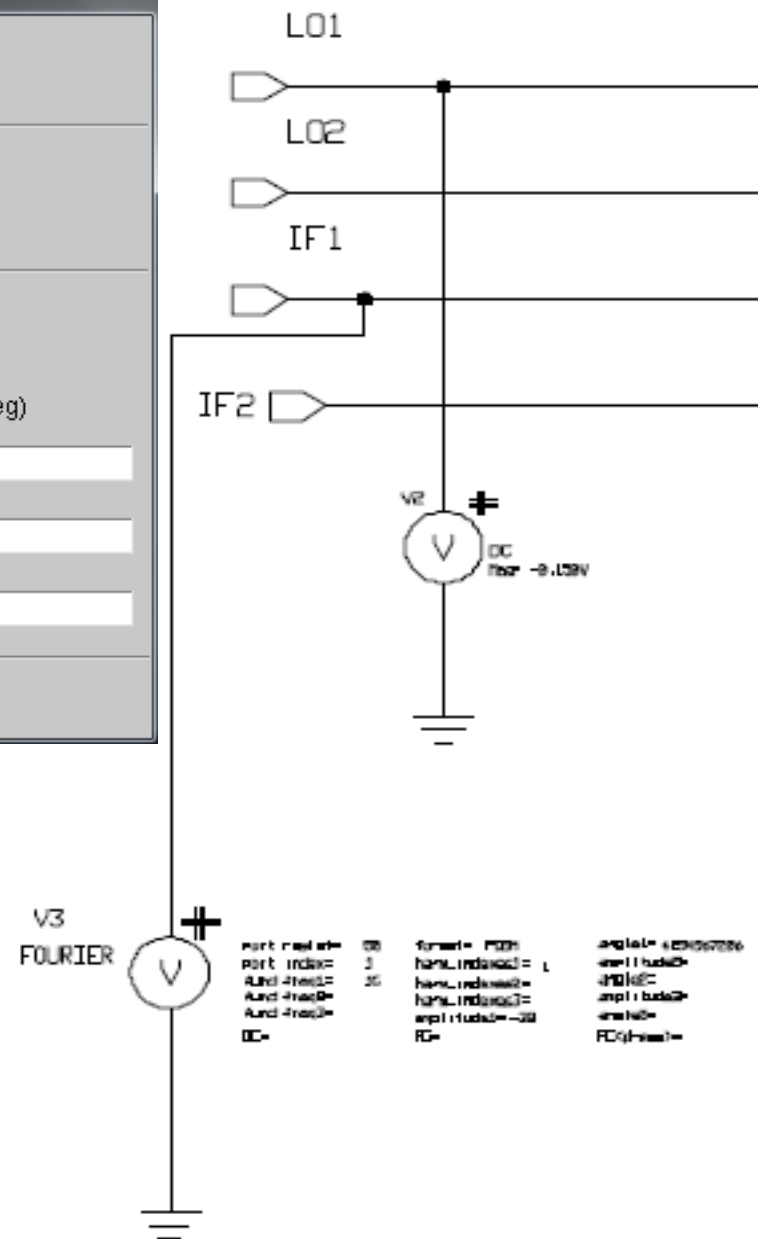
Port Index: Port Resistance:

Port Capacitance: Port Inductance:

Source Specification Format:
 MA RI DB PDB PDBM PMA

Tones	Intermodulation Index	Power(DBm)	Angle(Deg)	
1	1G	1	-30	-90
2				
3				

OK Reset Cancel





Overenie správnej funkčnosti návrhu

Check- horná lišta

Check list:

Warnings

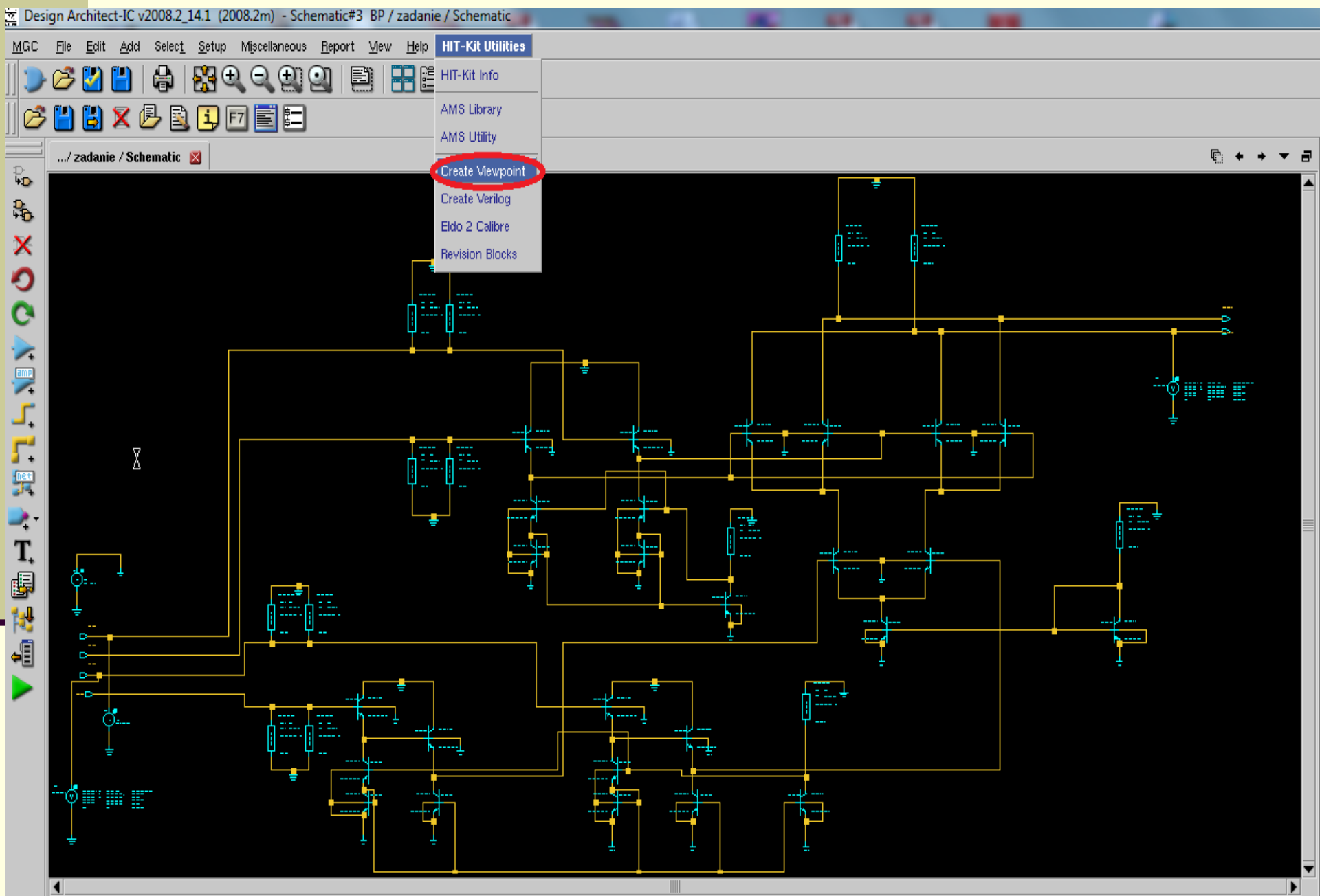
Errors -> nutné odstrániť

The screenshot shows a software interface with a menu bar (File, Edit, View, Window, Setup, Help) and a toolbar. The main window displays a report titled "zadanie.Report" with the following content:

```
Check Schematic "zadanie/schematic/sheet1"
Check Sheet "zadanie/schematic/sheet1"
Check SymbolPins ----- 0 errors 0 warnings (MGC-required)
Check Overlap ----- 0 errors 0 warnings
Check NotDots ----- 0 errors 0 warnings
Check Closedots ----- 0 errors 0 warnings
Check Dangle ----- 0 errors 0 warnings
Check UserRule ----- 0 errors 0 warnings
Check Function Blocks --- 0 errors 0 warnings
Check Instance ----- 0 errors (MGC-required)
Check Special ----- 0 errors 0 warnings (MGC-required)
Check Net ----- 0 errors 40 warnings (MGC-required)
Warning: Named net "vsub" (N$178) is shorted to Global "VEE" at I$68
Warning: Named net "vsub" (N$45) is shorted to Global "VEE" at I$23
Warning: Named net "vsub" (N$39) is shorted to Global "VEE" at I$24
Warning: Named net "vsub" (N$108) is shorted to Global "VEE" at I$49
Warning: Named net "vsub" (N$117) is shorted to Global "VEE" at I$50
Warning: Named net "vsub" (N$121) is shorted to Global "VEE" at I$52
Warning: Named net "L01" (N$221) is shorted to Global "ground" at I$100
Warning: Named net "vsub" (N$49) is shorted to Global "VEE" at I$25
Warning: Named net "vsub" (N$208) is shorted to Global "VEE" at I$31
Warning: Named net "vsub" (N$190) is shorted to Global "VEE" at I$79
Warning: Named net "vsub" (N$174) is shorted to Global "VEE" at I$73
Warning: Named net "vsub" (N$133) is shorted to Global "VEE" at I$60
Warning: Named net "vsub" (N$240) is shorted to Global "VEE" at I$87
Warning: Named net "vsub" (N$247) is shorted to Global "VEE" at I$28
Warning: Named net "vsub" (N$182) is shorted to Global "VEE" at I$76
Warning: Named net "vsub" (N$155) is shorted to Global "VEE" at I$77
Warning: Named net "vsub" (N$129) is shorted to Global "VEE" at I$59
Warning: Named net "vsub" (N$69) is shorted to Global "VEE" at I$34
Warning: Named net "vsub" (N$70) is shorted to Global "VEE" at I$35
Warning: Named net "vsub" (N$56) is shorted to Global "VEE" at I$29
Warning: Named net "vsub" (N$178) is shorted to Global "VEE" at I$68
Warning: Named net "vsub" (N$45) is shorted to Global "VEE" at I$23
Warning: Named net "vsub" (N$39) is shorted to Global "VEE" at I$24
Warning: Named net "vsub" (N$108) is shorted to Global "VEE" at I$49
Warning: Named net "vsub" (N$117) is shorted to Global "VEE" at I$50
Warning: Named net "vsub" (N$121) is shorted to Global "VEE" at I$52
```

On the right side of the interface, there is a vertical toolbar with buttons for "Open", "Schematic", "Symbol", "Setup", "Display", "Property Display", "Report", "Check Schematic", "Check Symbol", "Print", and "Session".

Simulácia- vytvorenie „Viewpoint“



Simulácia- vytvorenie „Viewpoint“

Design Architect-IC v2008.2_14.1 (2008.2m) - Schematic#3 BP / zadanie / Schematic

MGC File Edit Add Select Setup Miscellaneous Report View Help **HIT-Kit Utilities**

- HIT-Kit Info
- AMS Library
- AMS Utility
- Create Viewpoint**
- Create Verilog
- Eldo 2 Calibre
- Revision Blocks

.../zadanie / Schematic

Mentor Graphics

austriamicrosystems - DVE

Design Path Navigator...

Technology Name

Viewpoint Level

Extension to viewpoint name:

Simulácia- vytvorenie „Viewpoint“

The image shows a screenshot of the Design Architect-IC v2008.2_14.4 software interface. The main window displays a schematic diagram of a circuit. A dialog box titled "Entering Simulation Mode" is open in the foreground, showing a list of "Existing Configurations" with "vpt_s35d4_device_ams" selected and circled in red. The dialog box also includes options for "New Configuration...", "Save/Close Sheets in Current Design Only", "Re-initialize Configuration", "Cleanup Configuration References Upon Exit", and "Do Not Show This Dialog Again". The circuit schematic in the background shows a network of components including a resistor labeled "R1", a capacitor labeled "C1", and a diode labeled "NPN232". The circuit is connected to a power supply labeled "VEE". The software interface includes a menu bar (MGC, File, Edit, Add, Select, Setup, Miscellaneous, Report, View, Help), a toolbar, and a message area at the bottom.

Design Architect-IC v2008.2_14.4 (2008.2m p201106108) - Schematic#1 seminar / pokus1 / Schematic

Existing Configurations:

- Design Config
- vpt_s35d4_device_ams**

New Configuration...

Save/Close Sheets in Current Design Only

Re-initialize Configuration

Cleanup Configuration References Upon Exit

Do Not Show This Dialog Again

OK Reset Cancel

Message Area

Note: Reading version 26 of sheet \$seminar/default.group.logic.views/pokus1/schematic/sheet1
Note: austriamicrosystems 'HIT-Kit Utilities' menu added
Note: HIT-Kit Version 3.70, Copyright (c) austriamicrosystems AG, 1991-2005

Message Area

Note: Opening \$seminar/default.group.logic.views/pokus1/schematic/sheet1
Note: Reading version 26 of sheet \$seminar/default.group.logic.views/pokus1/schematic/sheet1
Note: Command file \$seminar/default.group.logic.views/pokus1/vpt_s35d4_device_ams.cir written.

Simulácia- výber modelov

The screenshot shows the Design Architect-IC v2008.2_14.4 software interface. The main window displays a circuit schematic with components like RPOLYB, NPN232, and AREA=12. A text overlay in the center-left of the schematic area provides instructions in Slovak. The top menu bar has 'HIT-Kit Utilities' circled in red. The left toolbar has a green play button circled in red. A dialog box titled 'Mentor Graphics austriamicrosystems - Model Parameter Selection' is open in the foreground, with the title bar circled in red. The dialog shows various parameter selection options for Cmos, Capacitor, Resistor, Inductor, and Bipolar components.

V simulačnom prostredí musíme nastaviť prvky, ktoré budú použité z knižnice *HIT-Kit Utilities*.

V hornej lište: *HIT-Kit Utilities* → *Set Simulation Models*.

Zvoliť všetky parametre *Typical* a *OK*.

Message Area:
Note: Reading version 28 of sheet \$seminar/default.group/logic/views/pokus1/schematic/sheet1
Warning: Sheet has not been checked successfully
Note: Command file \$seminar/default.group/logic/views/pokus1/vpt_s35d4_device_ams/pokus1_vpt_s35d4_device_ams_simulation_setup_form();

Log IC Station Simulation

Simulácia ► Setup Analysis



Setup Simulation Analysis

Click on the box to the left of the analysis to Enable or Disable

<input checked="" type="checkbox"/> DCOP	Setup...	<input type="checkbox"/> SST	Setup...
<input type="checkbox"/> DC	Setup...	<input type="checkbox"/> SST Oscil	Setup...
<input checked="" type="checkbox"/> AC	Setup...	<input type="checkbox"/> MODSST	Setup...
<input type="checkbox"/> Noise	Setup...	<input type="checkbox"/> SSTNoise	Setup...
<input type="checkbox"/> Transient	Setup...	<input type="checkbox"/> SSTAC	Setup...
<input type="checkbox"/> NoiseTran	Setup...		

OK Reset Cancel Help

Setup AC Analysis

Start freq.: 10MEG Stop freq.: 12G

Sweep: Decade Octave Linear

Points per Decade: 10 Points per Octave: 10 Number of points: 10

Use file name: _____

IC Nodeset

Initial conditions (-UIC)

Pole-Zero Setup:
 Locate the Poles and Zeros in the circuit

Output is:
 Current Through a Voltage Source
 Voltage Difference Between Two Nodes

Voltage Source: V3 Net 1: _____
Net 2 (difference): _____

Safe Operating Area Check SOA Autostop Add Checks...

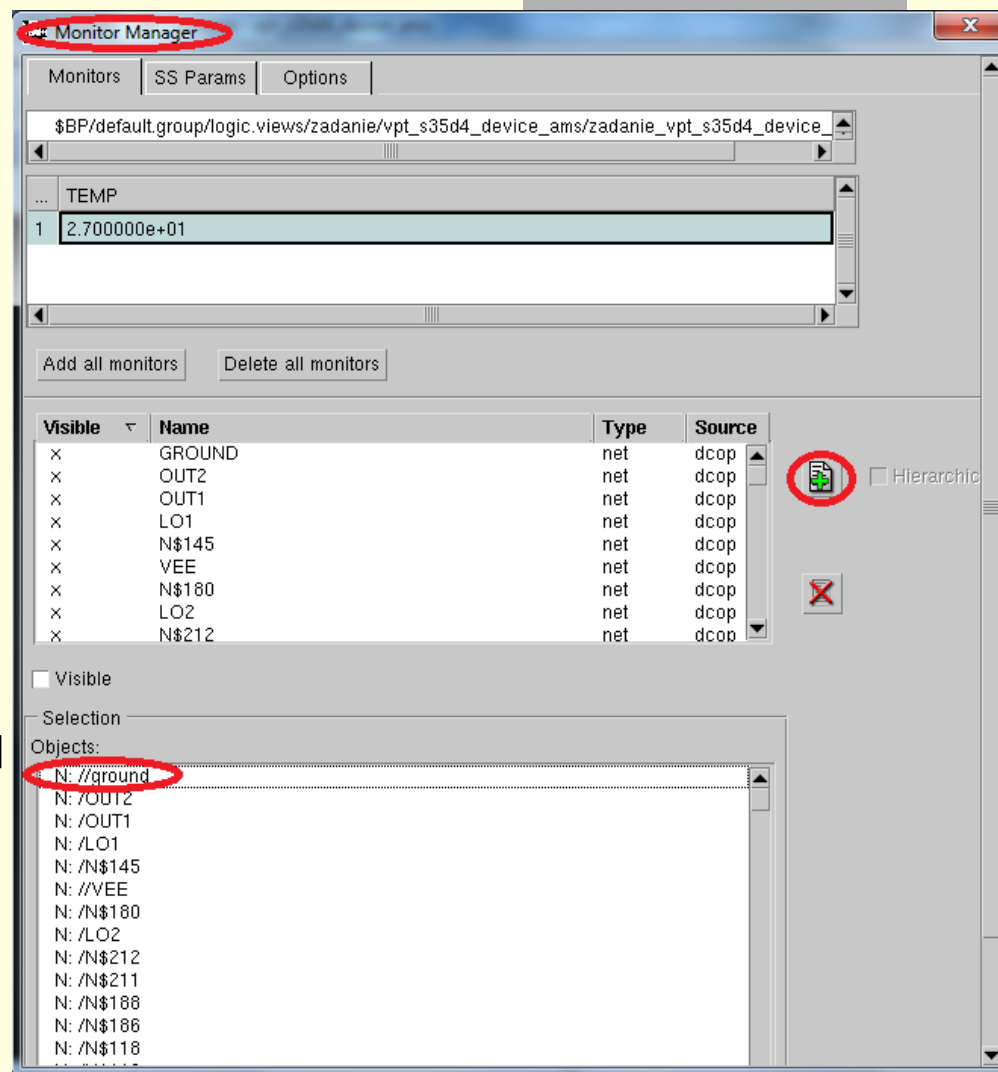
OK Reset Cancel Help

Simulácia -> nastavenie vykreslenia napätí a prúdov



Označíme celú schému obvodu a klikneme na **DCOP/TRAN**.

V obvode sa objavia hodnoty napätí a prúdov.



Simulácia -> Zobrazenie výstupov

Na vykreslenie priebehov, je potrebné nastaviť simulačné výstupy na **Wave Outputs**. Zvolíme *Edit Waveforms Analysis* → *All*, *Task* → *Save Only*, *Type* → *All (W, V, I, S)*, ...

Object	Analysis	Task	Type	Modifier	Harmonics
<input checked="" type="checkbox"/>	All	Save Only	All (W, V, I, S)	None	None

Analysis: All Harmonics: Use Parent's Harmonics

Task: Save Only File Name:

Type: All (W, V, I, S) Modifier: Magnitude, Magnitude (dB), Phase, Real, Imaginary, Group Delay

LIMPROBE Maximum Probes: 10000 Save

Simulácia -> Zobrazenie výstupov

Setup Simulation

Setup

- Library - Scenario
- Parameters - Sweeps
- Edit Forces
- Edit Waveforms**
- Corner Analysis
- MC Analysis

Object	Analysis	Task	Type	Modifier	Harmonics
<input checked="" type="checkbox"/>	All	Save Only	All (W, V, I, S)	None	None

Zvolíme *Edit Waveforms Analysis* → *All*, *Task* → *Save Only*, *Type* → *All (W, V, I, S)*, *Modifier* → *Magnitude* a *Maximum Probes* → *10000*.

Setup Net Highlight...

Probe All Currents Probe All Voltages

Analysis: All Harmonics: Use Parent's Harmonics

Task: Save Only File Name:

Type: All (W, V, I, S) Modifier: Magnitude

Top level Recursive levels: Differential

LIMPROBE Maximum Probes: 10000 Save

Wave Outputs

Simulácia -> Zobrazenie výstupov

Potvrdíme cez zelené plus, Add Wave Output !

Object	Analysis	Task	Type	Modifier	Harmonics
<input checked="" type="checkbox"/>	All	Save Only	All (W, V, I, S)	None	None

Setup Simulation

Setup

- Library - Scenario
- Parameters - Sweeps
- Edit Forces
- Edit Waveforms**
- Corner Analysis
- MC Analysis

End Sim

Setup

Session

Lib/Temp/Inc

Analyses...

Parameters...

Forces

Safe Operating Area

Options

Multiple Runs

Wave Outputs

Measurements

Model Selector

Execute

Setup Net Highlight...

Probe All Currents

Probe All Voltages

Analysis: All

Harmonics: Use Parent's Harmonics

Task: Save Only

File Name:

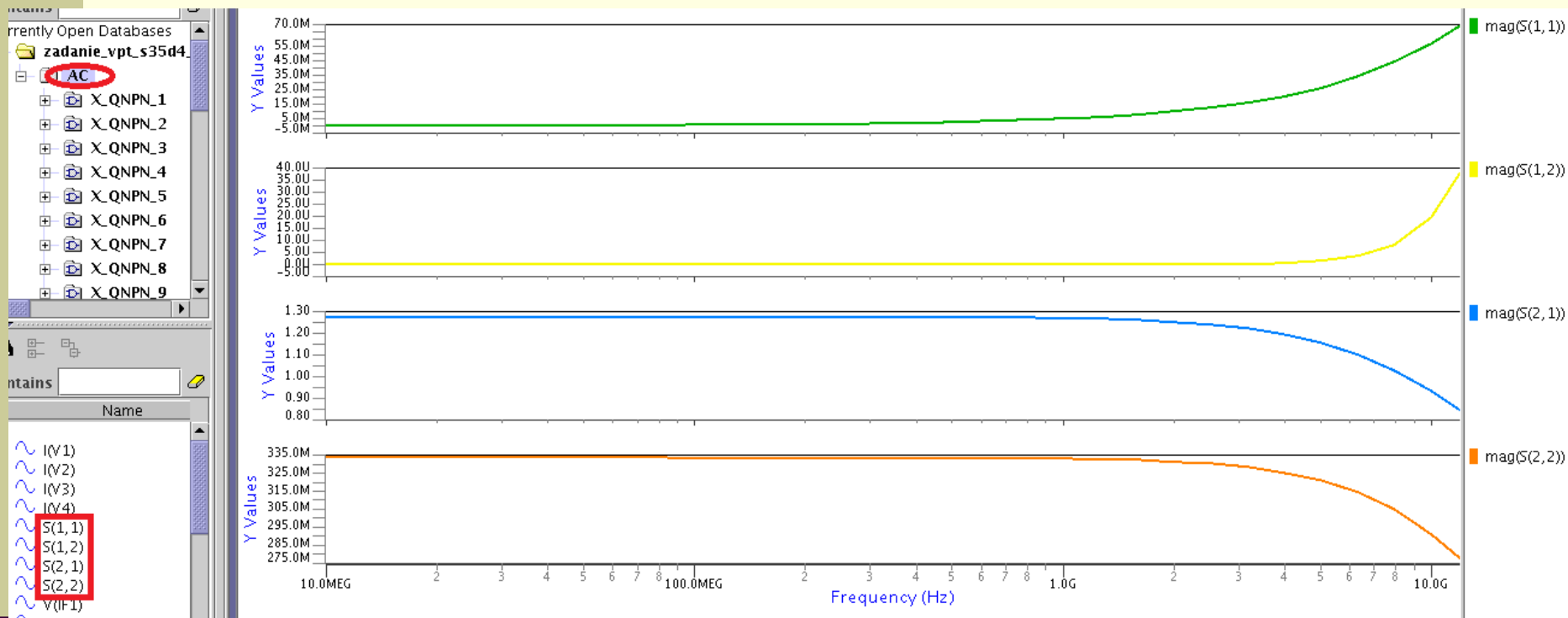
Type: All (W, V, I, S)

Modifier: Magnitude, Magnitude (dB), Phase, Real, Imaginary, Group Delay

LIMPROBE Maximum Probes: 10000

Save

Simulácia -> Vykreslenie simulácií



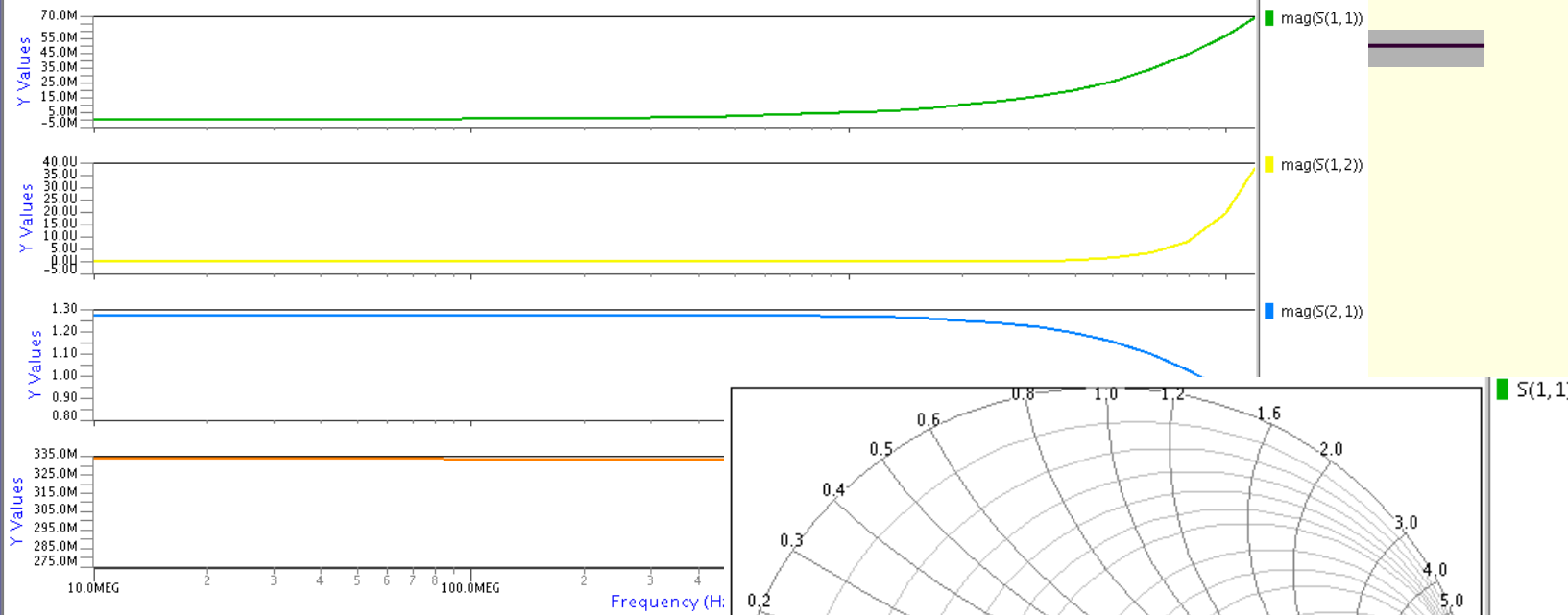
Vľavo dole *View Outputs*, ktorý nám umožňuje vykreslenie jednotlivých priebehov v rôznych jednotkách, alebo diagramoch, ako napríklad v Smithov-om diagrame.

S parameter- ponuka *Plot as* → *db, magnitude, real, smith_chart*

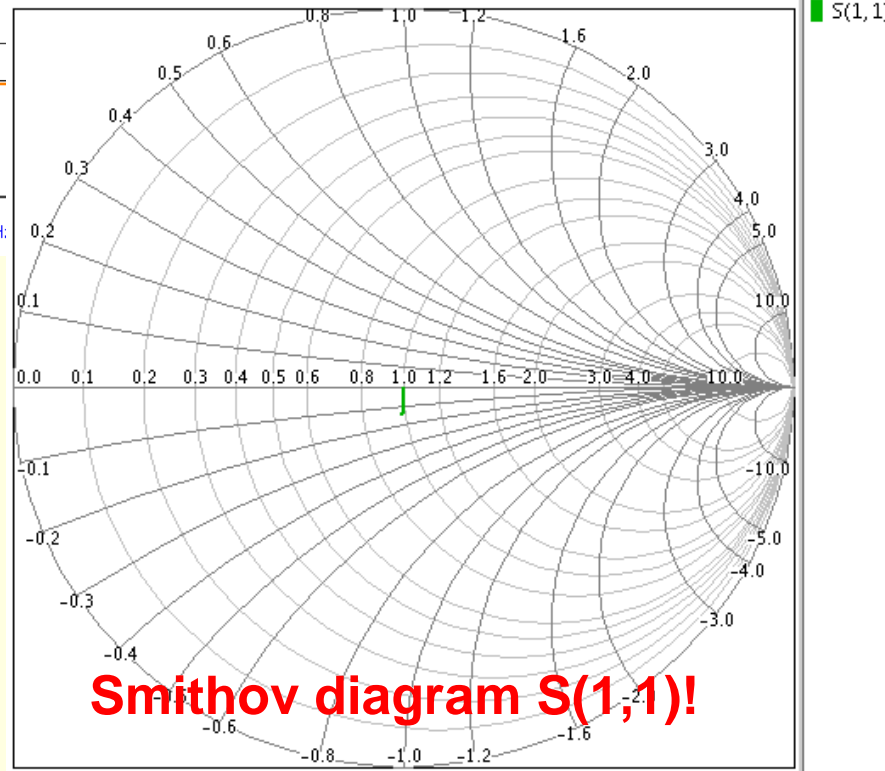
Simulácia -> Vykreslenie simulácií

Currently Open Databases
zadanie_vpt_s35d4
AC
X.QNPN_1
X.QNPN_2
X.QNPN_3
X.QNPN_4
X.QNPN_5
X.QNPN_6
X.QNPN_7
X.QNPN_8
X.QNPN_9

contains
Name
I(V1)
I(V2)
I(V3)
I(V4)
S(1,1)
S(1,2)
S(2,1)
S(2,2)
V(I,F1)



End Sim Mode:
Zo **simulačného** prostredia
do **návrhového**



Vytlačenie -> schémy

Hlavná lišta *Print*

Print Name → *PDF*

Veľkosť strany → požadovaný formát

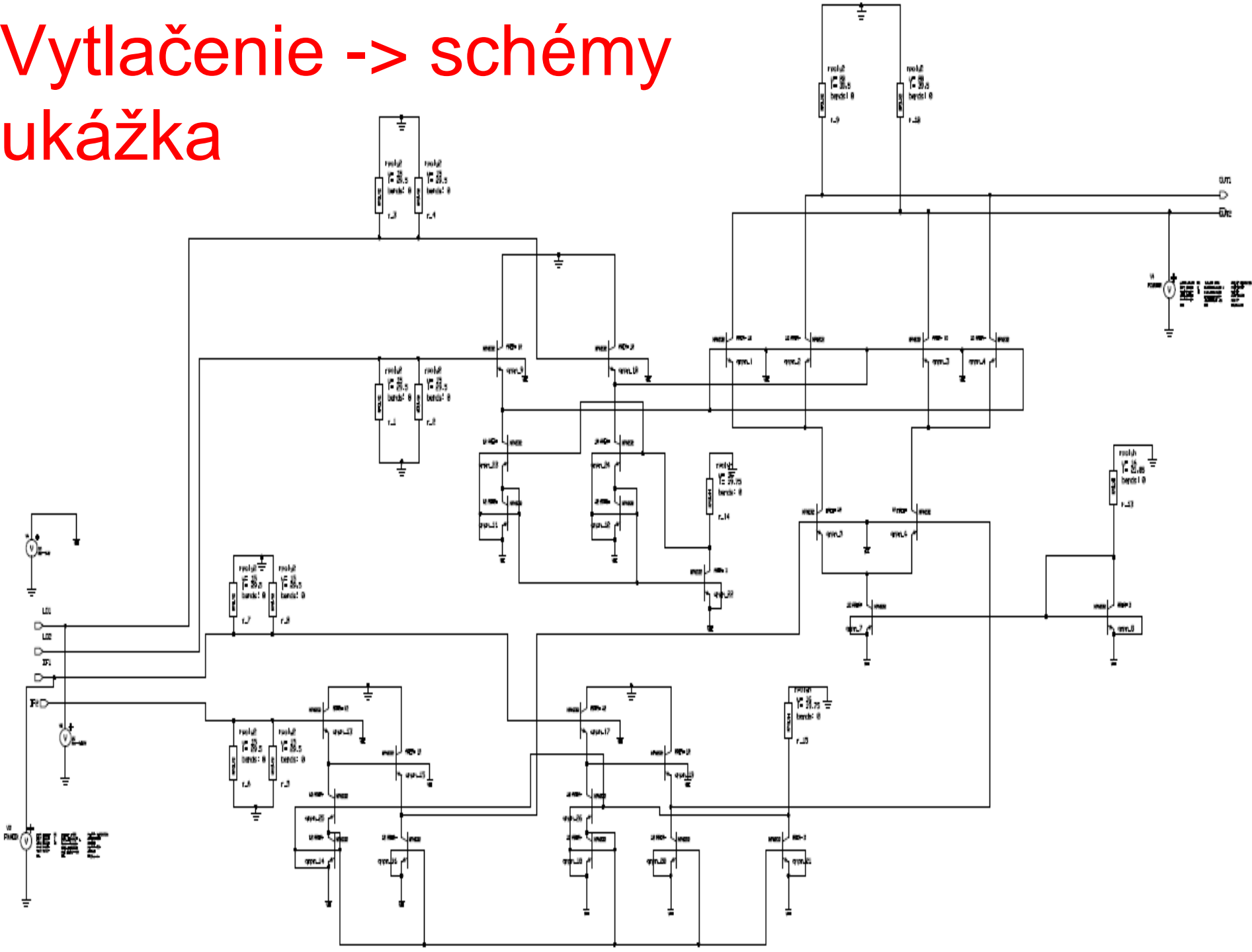
Necháme *Rotation* → *Best Fit*

Output Format → *Basic PostScript*

Color → *Monochrome* (pre lepšiu čitateľnosť)

Schéma sa uloží v domovskom priečinku

Vytlačenie -> schémy ukážka



Layout- morfológia masiek

The image shows a screenshot of the IC Station v2008.2.14.3 software interface. The main window displays a PCB layout design with various components and traces. The title bar indicates the file path: "IC Station v2008.2.14.3 (2008.2m p... 01106058) - IC 0: pokus1 > pokus1 (i)". The menu bar includes options like MGC, File, Context, Objects, Edit, Select, Connect, Routing, Setup, Report, Other, View, Change, Translate, Packages, Calltree, Help, HIT-Kit Utilities, and Show LP. The toolbar contains icons for various functions. The left sidebar lists editing tools such as Easy Edit, Edit, Expert Edit, CBC Edit, DLA Layout, DLA Device, ECO, IC Session, ICrules, Instant DRC, Short Checker, ITrace (D), ITrace (M), Verifdp (DRC), Verifdp (LVS), ICassemble, Plan & Place, Route, ICBlocks, Floorplan, and Place & Route. The right sidebar shows the Layer Palette with a list of layers and their properties. The bottom status bar displays the Message Area with notes: "Note: Cell 'pokus1' reserved for edit.", "Note: Setting window grid", and "Note: HIT-Kit Version 3.70, Copyright (c) austriamicrosystems AG, 1991-2005". The taskbar at the bottom shows several open windows, including "ICStudio - Project tukeic" and "IC Station". A red circle highlights the "Layout" option in the "ICStudio - Project tukeic" window's menu.

IC Station v2008.2.14.3 (2008.2m p... 01106058) - IC 0: pokus1 > pokus1 (i)

MGC File Context Objects Edit Select Connect Routing Setup Report Other View Change Translate Packages Calltree Help HIT-Kit Utilities Show LP

Context: pokus1(GE-E 0) Process: s35d4(-R) Dynamic Status: Cursor: 82.750 10.500 Layer: NBUR Sel: 0 Hotkeys: off

Layer Palette

Layer	Color	Material
NBUR	Black	svf
s35d4	Black	svf
AS	Black	AF
AV	Black	AF
AF	Black	AF
NBUR	Black	svf
PBUEF	Black	svf
TRENCH	Black	svf
NTUB	Black	svf
FIMP	Black	svf
DIFF	Black	svf
COLL	Black	svf
MIDOX	Black	svf
BNTUB	Black	svf
BNTUB2	Black	svf
POLY1	Black	svf
NLDD	Black	svf
PLDD	Black	svf
NPLUS	Black	svf
PPLUS	Black	svf
HBT	Black	svf
EMITT	Black	svf
BPOLY	Black	svf
HRES	Black	svf
POLY2	Black	svf
SALEX	Black	svf
EPOLY	Black	svf
CONT	Black	svf
MET1	Black	svf
VIA1	Black	svf
MET2	Black	svf
VIA2	Black	svf
MET3	Black	svf
PAD	Black	svf
VIA3	Black	svf
MET4	Black	svf
LVTA	Black	svf

Message Area

Note: Cell "pokus1" reserved for edit.
Note: Setting window grid
Note: HIT-Kit Version 3.70, Copyright (c) austriamicrosystems AG, 1991-2005

[Downloads - File Brow... [mc [palo@KaktusDe... [TUKE -- TUKE - icewe... ICStudio - Project tukeic IC Station

Layout

```
%%close_window(@discard, void, @false);  
$set_active_window("session");  
$set_active_window("session");  
$close_session(void);
```

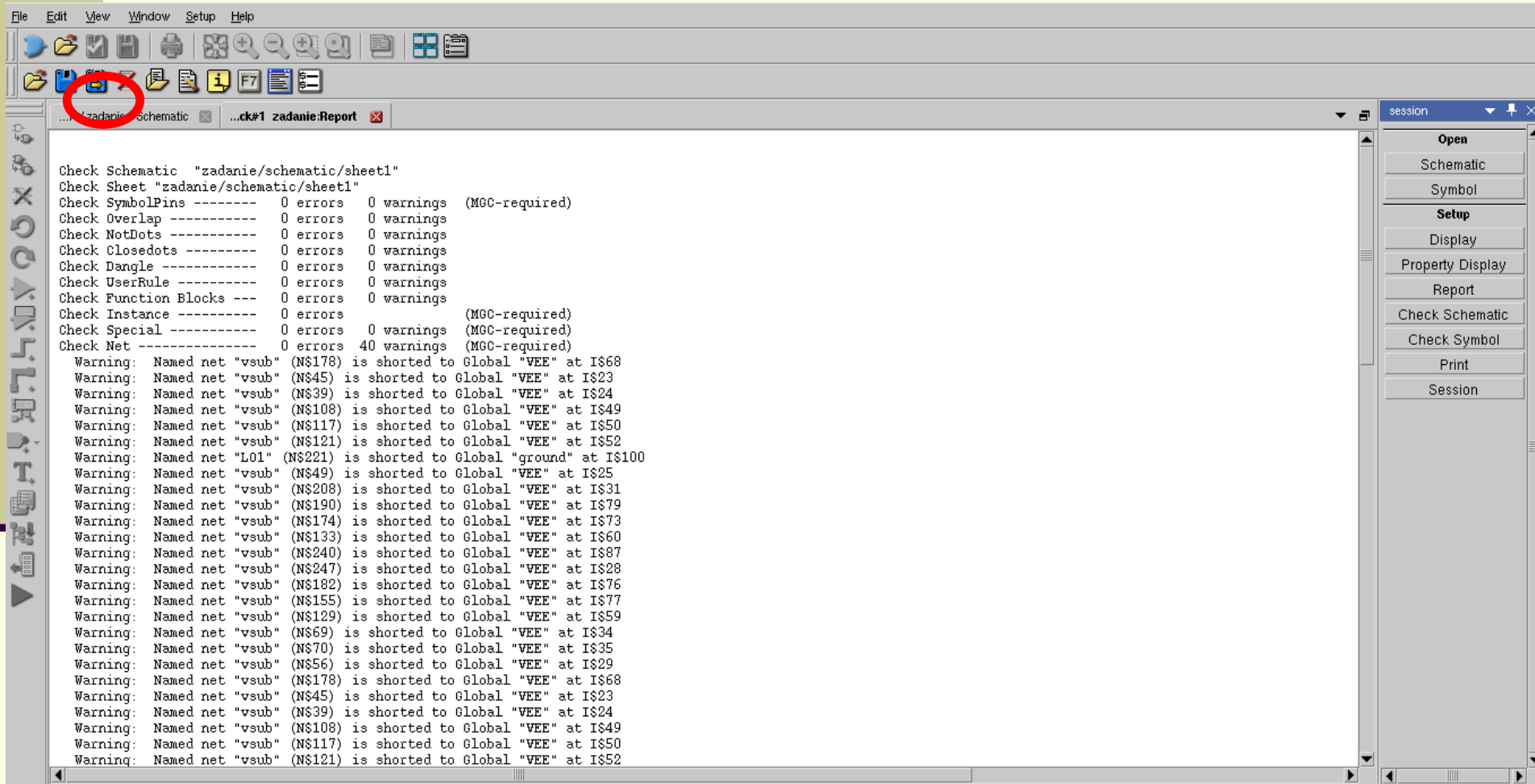
Symbol

The image displays four overlapping windows of the Design Architect-IC v2008.2.14.4 software, showing different schematic sheets for a mixer circuit.

- Schematic#3 (top-left):** Shows a high-level schematic with a central component labeled `MIX_1_042`. It has two input ports (`IN1`, `IN2`) and two output ports (`OUT1`, `OUT2`). The component is connected to a voltage source `0_022` and a resistor.
- Schematic#4 (top-right):** Shows a circular symbol for the `MIX_1_042` component. The symbol is divided into four quadrants labeled `IF1`, `IF2`, `OUT1`, and `OUT2`. It also features two pins labeled `L01` and `L02`. The view is set to `VIEW=$Default()`.
- Schematic#5 (bottom-left):** Shows a detailed schematic of the mixer's internal structure, featuring a series of resistors (`rpolu1` to `rpolu8`) and operational amplifiers (`opam1` to `opam8`) arranged in a complex network.
- Schematic#6 (bottom-right):** Shows a detailed schematic of the mixer's internal structure, featuring a series of resistors (`rpolu1` to `rpolu8`) and operational amplifiers (`opam1` to `opam8`) arranged in a complex network.

The software interface includes a menu bar (MGC, File, Edit, Add, Select, Setup, Miscellaneous, Report, View, Help), a toolbar, and a right-hand panel with various tool options like Session, Draw, Text, Check & Save, Select, Edit, Move, Copy, Delete, Undo, Sketch, Fill, Add, Pin, Polyline, Polygon, Rectangle, Arc, Circle, and Miscellaneous. The bottom status bar shows the current sheet name and version information.

Overenie správnej funkčnosti návrhu



The screenshot shows a software interface with a menu bar (File, Edit, View, Window, Setup, Help) and a toolbar. A red circle highlights a button in the toolbar. The main window displays a report titled "ck#1 zadanie:Report" with the following content:

```
Check Schematic "zadanie/schematic/sheet1"
Check Sheet "zadanie/schematic/sheet1"
Check SymbolPins ----- 0 errors 0 warnings (MGC-required)
Check Overlap ----- 0 errors 0 warnings
Check NotDots ----- 0 errors 0 warnings
Check Closedots ----- 0 errors 0 warnings
Check Dangle ----- 0 errors 0 warnings
Check UserRule ----- 0 errors 0 warnings
Check Function Blocks --- 0 errors 0 warnings
Check Instance ----- 0 errors 0 warnings (MGC-required)
Check Special ----- 0 errors 0 warnings (MGC-required)
Check Net ----- 0 errors 40 warnings (MGC-required)
Warning: Named net "vsub" (N$178) is shorted to Global "VEE" at I$68
Warning: Named net "vsub" (N$45) is shorted to Global "VEE" at I$23
Warning: Named net "vsub" (N$39) is shorted to Global "VEE" at I$24
Warning: Named net "vsub" (N$108) is shorted to Global "VEE" at I$49
Warning: Named net "vsub" (N$117) is shorted to Global "VEE" at I$50
Warning: Named net "vsub" (N$121) is shorted to Global "VEE" at I$52
Warning: Named net "L01" (N$221) is shorted to Global "ground" at I$100
Warning: Named net "vsub" (N$49) is shorted to Global "VEE" at I$25
Warning: Named net "vsub" (N$208) is shorted to Global "VEE" at I$31
Warning: Named net "vsub" (N$190) is shorted to Global "VEE" at I$79
Warning: Named net "vsub" (N$174) is shorted to Global "VEE" at I$73
Warning: Named net "vsub" (N$133) is shorted to Global "VEE" at I$60
Warning: Named net "vsub" (N$240) is shorted to Global "VEE" at I$87
Warning: Named net "vsub" (N$247) is shorted to Global "VEE" at I$28
Warning: Named net "vsub" (N$182) is shorted to Global "VEE" at I$76
Warning: Named net "vsub" (N$155) is shorted to Global "VEE" at I$77
Warning: Named net "vsub" (N$129) is shorted to Global "VEE" at I$59
Warning: Named net "vsub" (N$69) is shorted to Global "VEE" at I$34
Warning: Named net "vsub" (N$70) is shorted to Global "VEE" at I$35
Warning: Named net "vsub" (N$56) is shorted to Global "VEE" at I$29
Warning: Named net "vsub" (N$178) is shorted to Global "VEE" at I$68
Warning: Named net "vsub" (N$45) is shorted to Global "VEE" at I$23
Warning: Named net "vsub" (N$39) is shorted to Global "VEE" at I$24
Warning: Named net "vsub" (N$108) is shorted to Global "VEE" at I$49
Warning: Named net "vsub" (N$117) is shorted to Global "VEE" at I$50
Warning: Named net "vsub" (N$121) is shorted to Global "VEE" at I$52
```

The right sidebar contains a "session" dropdown and a list of buttons: Open, Schematic, Symbol, Setup, Display, Property Display, Report, Check Schematic, Check Symbol, Print, and Session.

Europpractice IC mission

- **Prototyping**
- Multi Project Wafer Runs (MPWs)
- Design Kits
- Prototype testing
- Prototype encapsulations (packaging)
- EDA support

<http://www.europpractice-ic.com/prototyping.php>

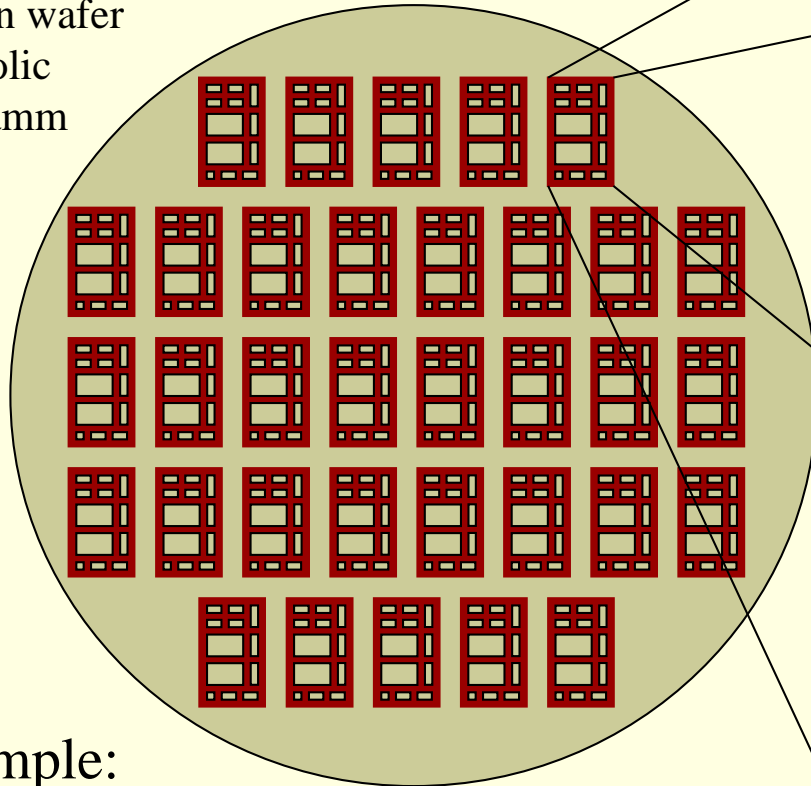
- **Volume Production**
- Low cost after prototype fabrication service
- Packaging and tests
- ASIC qualification
- Technical support



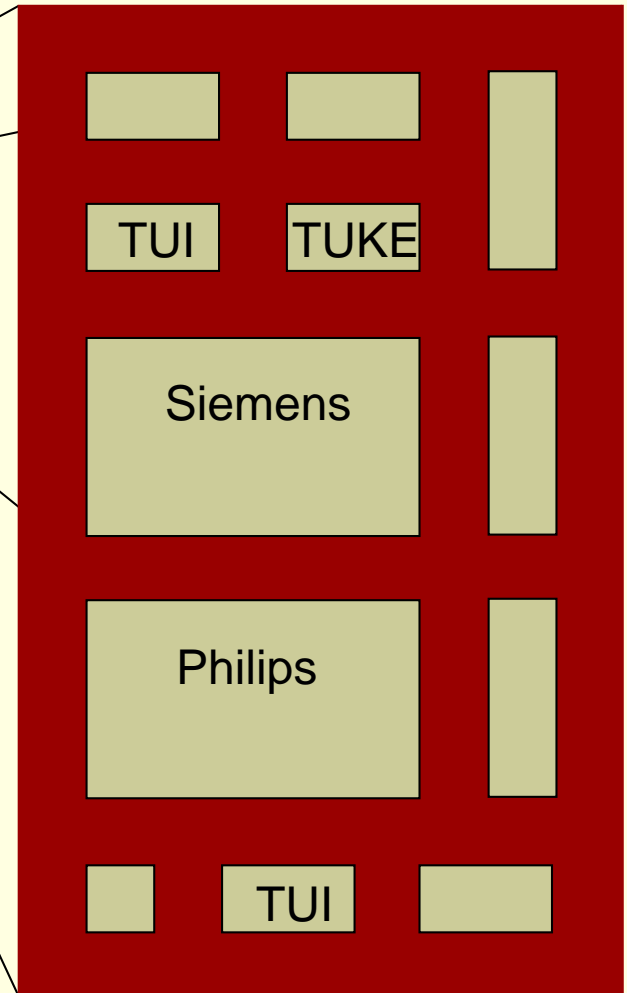
http://www.europpractice-ic.com/volume_production.php

MPW ~ multi-project wafer

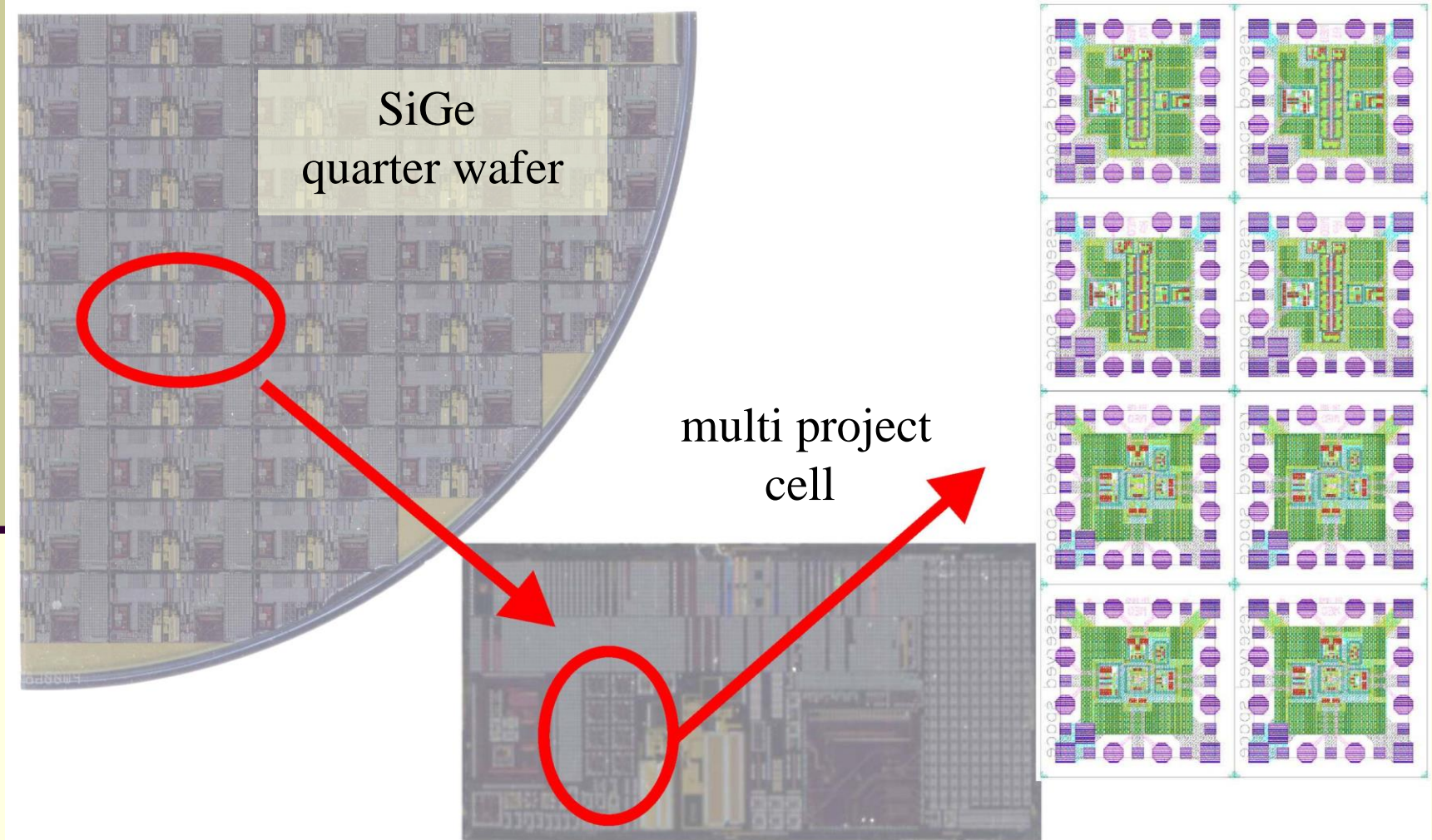
Silicon wafer
symbolic
diagramm



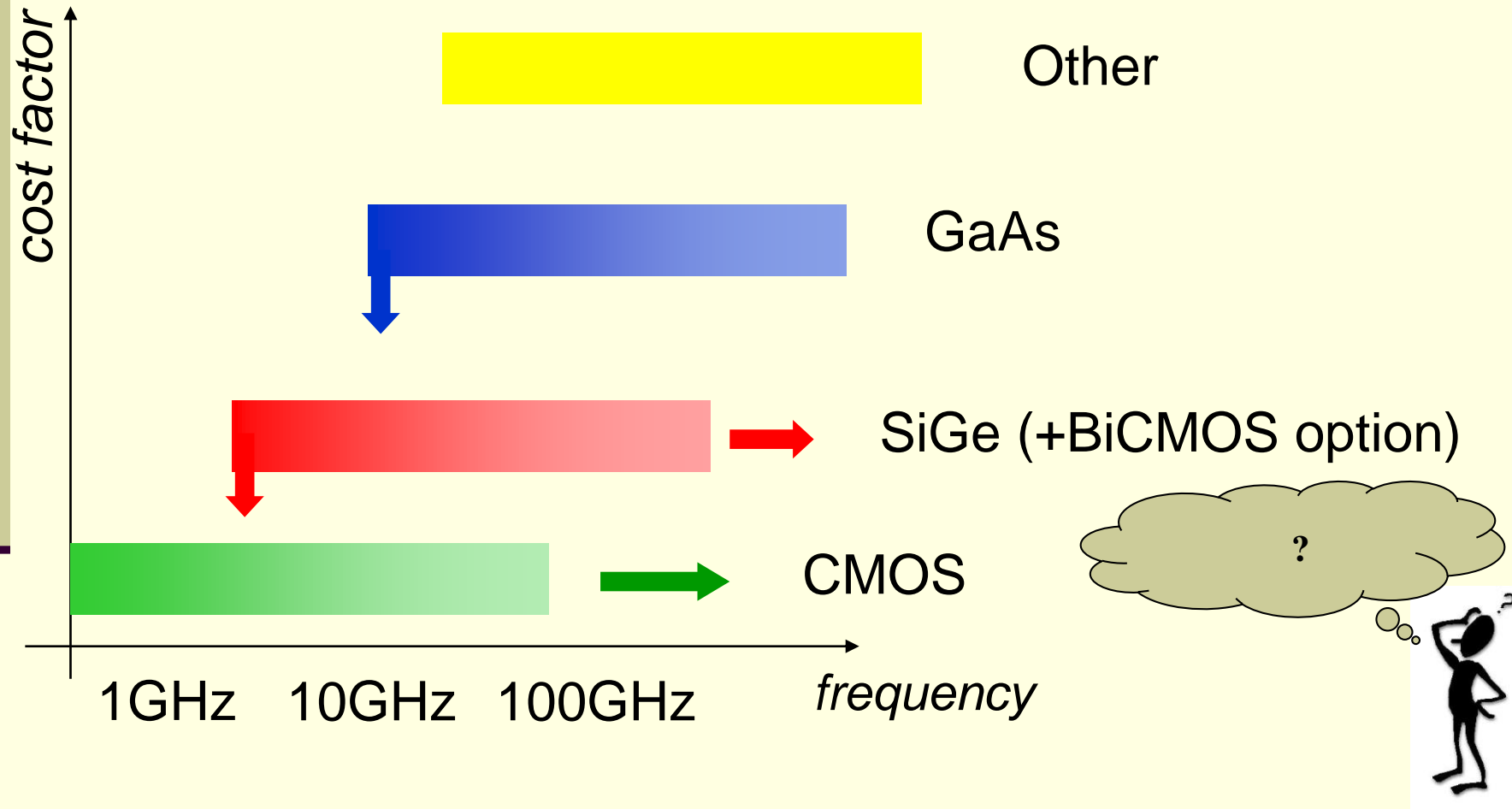
Example:
MPW organisation



MPW ~ prototyping example



IC technology aspects



Other considerations: **SNR** (SiGe), **Linearity** (CMOS), **Modelling** (SiGe) ...

EU MPW available technologies



CMOS - 0,8 μ m; 0,35 μ m; 0,18 μ m
BiCMOS - 0,35 μ m



CMOS - 0,7 μ m; 0,5 μ m; 0,35 μ m



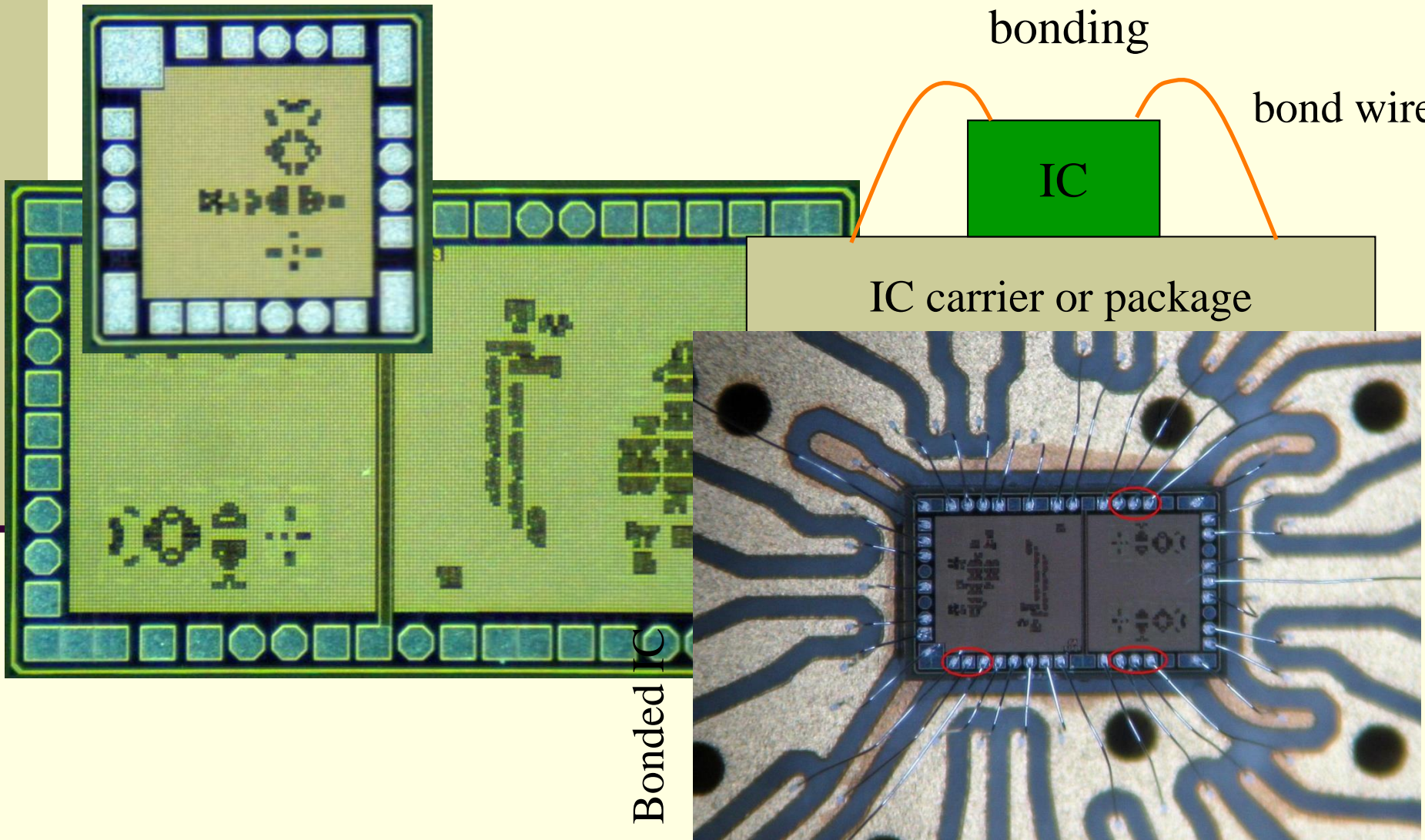
BiCMOS - 0,25 μ m; 0,13 μ m
(Ft up to 300GHz)



CMOS - 0,25 μ m; 0,13 μ m
(... 45nm)

*EUROPRACTICE SUPPORTED processes, selected technologies

Examples of IC prototypes



Examples of IC prototypes

