DR8051XP

High Performance Configurable 8-bit Microcontroller

ver 3.10

OVERVIEW

DR8051XP is a **high performance, area optimized** soft core of a single-chip 8-bit embedded controller dedicated for operation with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern about **low power consumption**. Additionally an advanced power management unit makes DR8051XP core **perfect for portable equipment** where low power consumption is mandatory.

DR8051XP soft core is 100% binary-compatible with the industry standard 8051 8-bit microcontroller. There are two configurations of DR8051XP: **Harward** where external data and program buses are separated, and **von Neumann** with common program and external data bus. DR8051XP has RISC architecture **6.7 times faster** compared to standard architecture and executes **65-200 million instructions** per second. This performance can also be exploited to great advantage in **low power** applications where the core can be clocked up to seven times more slowly than the original implementation for no performance penalty.

DR8051XP is **fully customizable**, which means it is delivered in the exact configuration to meet users' requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU KEY FEATURES

- 100% software compatible with industry standard 8051

- RISC architecture enables to execute instructions 6.7 times faster compared to standard 8051

- 12 times faster multiplication

- 9.6 times faster division

- 2 Data Pointers (DPTR) for faster memory blocks copying

  - *Advanced INC & DEC modes*

  - *Auto-switch of current DPTR*

- Up to 256 bytes of internal (on-chip) Data Memory

- Up to 64K bytes of Program Memory

- Up to 16M bytes of external (off-chip) Data Memory

- User programmable Program Memory Wait States solution for wide range of memories speed

- User programmable External Data Memory Wait States solution for wide range of memories speed

http://www.DigitalCoreDesign.com
http://www.dcd.pl

- De-multiplexed Address/Data bus to allow easy connection to memory
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready
- **1.3 GHz virtual** clock frequency in a 0.35u technological process

PERIPHERALS

- DoCD™ debug unit
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware breakpoints activated at a certain*
    - *Program address (PC)*
    - *Address by any write into memory*
    - *Address by any read from memory*
    - *Address by write into memory a required data*
    - *Address by read from memory a required data*
  - *Three wire communication interface*
- Power Management Unit
  - *Power management mode*
  - *Switchback feature*
  - *Stop mode*
- Extended Interrupt Controller
  - *2 priority levels*
  - *Up to 7 external interrupt sources*

- *Up to 8 interrupt sources from peripherals*
- Four 8-bit I/O Ports
  - *Bit addressable data direction for each line*
  - *Read/write of single line and 8-bit group*
- Three 16-bit timer/counters
  - *Timers clocked by internal source*
  - *Auto reload 8/16-bit timers*
  - *Externally gated event counters*
- Full-duplex serial port
  - *Synchronous mode, fixed baud rate*
  - *8-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, variable baud rate*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
  - *Interrupt generation*
- I2C bus controller - Slave
  - *NORMAL speed 100 kbs*
  - *FAST speed 400 kbs*
  - *HIGH speed 3400 kbs*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*
  - *Interrupt generation*
- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Four transfer formats supported*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- Programmable Watchdog Timer
- 16-bit Compare/Capture Unit
  - *Events capturing*

http://www.DigitalCoreDesign.com
http://www.dcd.pl

- *Pulses generation*
- *Digital signals generation*
- *Gated timers*
- *Sophisticated comparator*
- *Pulse width modulation*
- *Pulse width measuring*
- Fixed-Point arithmetic coprocessor
  - *Multiplication - 16bit * 16bit*
  - *Division - 32bit / 16bit*
  - *Division - 16bit / 16bit*
  - *Left and right shifting - 1 to 31 bits*
  - *Normalization*
- Floating-Point arithmetic coprocessor IEEE-754 standard single precision
  - *FADD, FSUB - addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM - compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
- Floating-Point math coprocessor - IEEE-754 standard single precision real, word and short integers
  - *FADD, FSUB- addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM- compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
  - *FSIN, FCOS- sine, cosine*
  - *FTAN, FATAN- tangent, arcs tangent*

Memory style	- Harward - von Neumann
Program Memory type	- synchronous - asynchronous
Program Memory wait-states	- used (0-7) - unused
Program Memory writes	- used - unused
Internal Data Memory type	- synchronous - asynchronous
External Data Memory wait-states	- used (0-7) - unused
Second Data Pointer (DPTR1)	- used - unused
Data Pointers decrement	- used - unused
Data Pointers auto-switch	- used - unused
Interrupts	- subroutines location
Timing access protection	- used - unused
Power Management Mode	- used - unused
Stop mode	- used - unused
DoCD™ debug unit	- used - unused

Besides mentioned above parameters all available peripherals and external interrupts can be excluded from the core by changing appropriate constants in package file.

CONFIGURATION

The following parameters of the DR8051XP core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

DELIVERABLES

- ◆ Source code:
  - ◊ VHDL Source Code or/and
  - ◊ VERILOG Source Code or/and
  - ◊ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
  - ◊ Active-HDL automatic simulation macros
  - ◊ ModelSim automatic simulation macros
  - ◊ Tests with reference responses
- ◆ Technical documentation
  - ◊ Installation notes
  - ◊ HDL core specification
  - ◊ Datasheet

http://www.DigitalCoreDesign.com
http://www.dcd.pl

- ♦ Synthesis scripts
- ♦ Example application
- ♦ Technical support
  - ◊ IP Core implementation support
  - ◊ 3 months maintenance
    - • Delivery the IP Core updates, minor and major versions changes
    - • Delivery the documentation updates
    - • Phone & email support

LICENSING

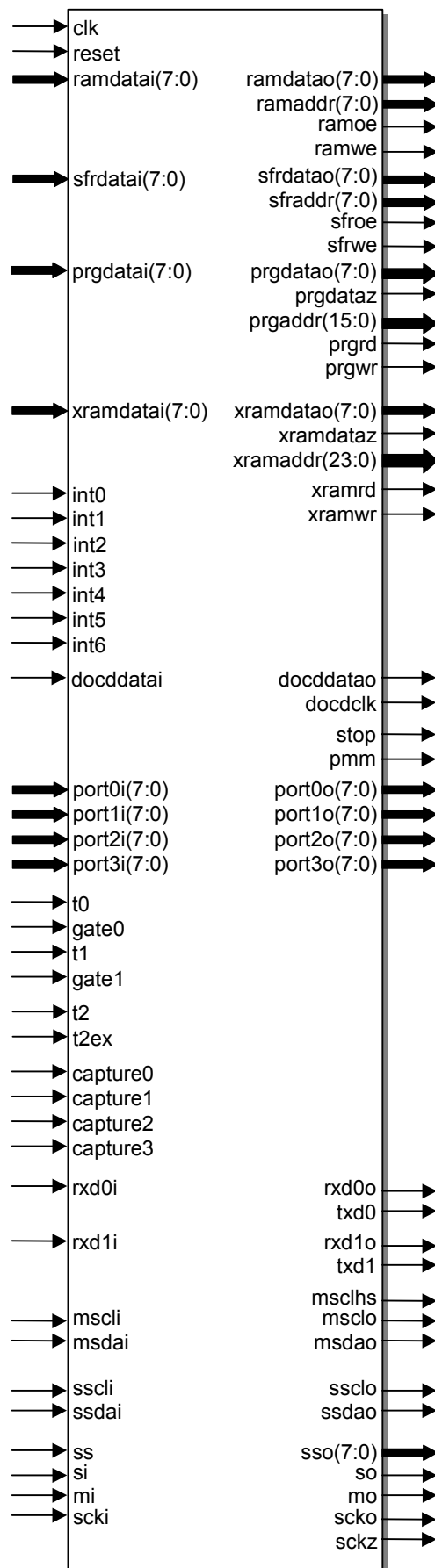Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- • Single Design license for
  - ○ *VHDL, Verilog source code called HDL Source*
  - ○ *Encrypted, or plain text EDIF called Netlist*
- • One Year license for
  - ○ *Encrypted Netlist only*
- • Unlimited Designs license for
  - ○ *HDL Source*
  - ○ *Netlist*
- • Upgrade from
  - ○ *HDL Source to Netlist*
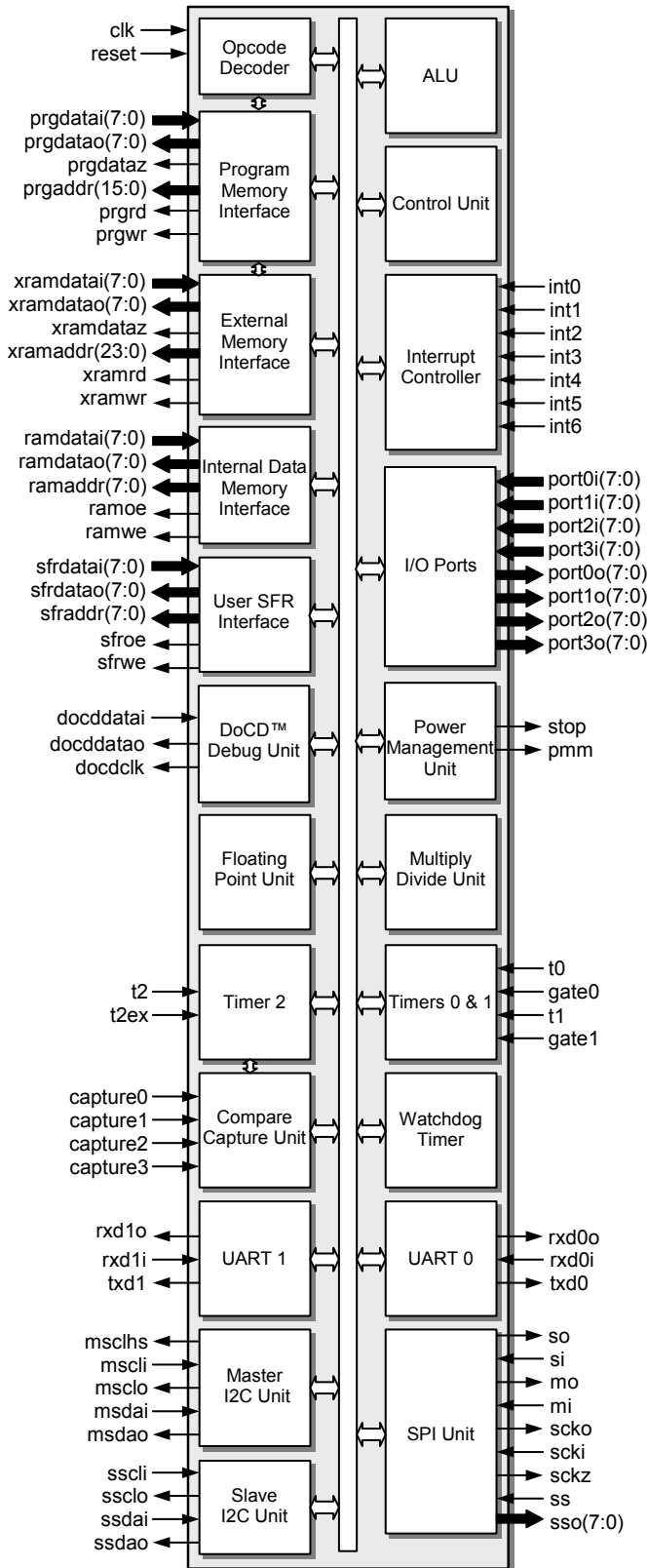 - ○ *Single Design to Unlimited Designs*

SYMBOL

Inputs	Outputs
clk	
reset	
ramdatai(7:0)	ramdatao(7:0)
	ramaddr(7:0)
	ramoe
	ramwe
sfrdatai(7:0)	sfrdatao(7:0)
	sfraddr(7:0)
	sfroe
	sfrwe
prgdatai(7:0)	prgdatao(7:0)
	prgdataz
	prgaddr(15:0)
	prgrd
	prgwr
xramdatai(7:0)	xramdatao(7:0)
	xramdataz
	xramaddr(23:0)
int0	xramrd
int1	xramwr
int2	
int3	
int4	
int5	
int6	
docddatai	docddatao
	docdclk
	stop
	pmm
port0i(7:0)	port0o(7:0)
port1i(7:0)	port1o(7:0)
port2i(7:0)	port2o(7:0)
port3i(7:0)	port3o(7:0)
t0	
gate0	
t1	
gate1	
t2	
t2ex	
capture0	
capture1	
capture2	
capture3	
rxd0i	rxd0o
	txd0
rxd1i	rxd1o
	txd1
	msclhs
mscli	msclo
msdai	msdao
sscli	ssclo
ssdai	ssdao
ss	sso(7:0)
si	so
mi	mo
scki	scko
	sckz

http://www.DigitalCoreDesign.com
http://www.dcd.pl

BLOCK DIAGRAM

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global synchronous reset
ramdatai[7:0]	input	Data bus from Internal Data Memory
sfrdatai[7:0]	input	Data bus from user SFRs
prgdatai[7:0]	input	Input data bus from Program Memory
xramdatai[7:0]	input	Data bus from External Data Memory
int0	input	External interrupt 0 line
int1	input	External interrupt 1 line
int2	input	External interrupt 2 line
int3	input	External interrupt 3 line
int4	input	External interrupt 4 line
int5	input	External interrupt 5 line
int6	input	External interrupt 6 line
docddatai	input	DoCD™ data input
port0i[7:0]	input	Port 0 input
port1i[7:0]	input	Port 1 input
port2i[7:0]	input	Port 2 input
port3i[7:0]	input	Port 3 input
t0	input	Timer 0 clock line
gate0	input	Timer 0 clock line gate control
t1	input	Timer 1 clock line
gate1	input	Timer 1 clock line gate control
t2	input	Timer 2 clock line
t2ex	input	Timer 2 control
capture0	input	Timer 2 capture 0 line
capture1	input	Timer 2 capture 1 line
capture2	input	Timer 2 capture 2 line
capture3	input	Timer 2 capture 3 line
rxd0i	input	Serial receiver input 0
rxd1i	input	Serial receiver input 1
mscli	input	Master I2C clock line input
msdai	input	Master I2C data input
sscli	input	Slave I2C clock line input
ssdai	input	Slave I2C data input
ss	input	SPI slave select
si	input	SPI slave input
mi	input	SPI master input
scki	input	SPI clock input
ramdatao[7:0]	output	Data bus for Internal Data Memory
ramaddr[7:0]	output	Internal Data Memory address bus
ramoe	output	Internal Data Memory output enable
ramwe	output	Internal Data Memory write enable
sfrdatao[7:0]	output	Data bus for user SFRs
sfraddr[7:0]	output	User SFRs address bus
sfroe	output	User SFRs output enable
sfrwe	output	User SFRs write enable
prgaddr[15:0]	output	Program Memory address bus

http://www.DigitalCoreDesign.com
http://www.dcd.pl

prgdatao[7:0]	output	Output data bus for Program Memory
prgdataz	output	PRGDATA tri-state buffers control line
prgrd	output	Program Memory read
prgwr	output	Program Memory write
xramdatao[7:0]	output	Data bus for External Data Memory
xramdataz	output	XDATA tri-state buffers control line
xramaddr[23:0]	output	External Data Memory address bus
xramrd	output	External Data Memory read
xramwr	output	External Data Memory write
docddatao	output	DoCD™ data output
docdclk	output	DoCD™ clock line
pmm	output	Power management mode indicator
stop	output	Stop mode indicator
port0o[7:0]	output	Port 0 output
port1o[7:0]	output	Port 1 output
port2o[7:0]	output	Port 2 output
port3o[7:0]	output	Port 3 output
rxd0o	output	Serial receiver output 0
txd0	output	Serial transmitter line 0
rxd1o	output	Serial receiver output 1
txd1	output	Serial transmitter line 1
msclo	output	Master I2C clock output
msclhs	output	High speed Master I2C clock line
msdao	output	Master I2C data output
msclo	output	Slave I2C clock output
msdao	output	Slave I2C data output
sso[7:0]	output	SPI slave select lines
so	output	SPI slave output
mo	output	SPI master output
scko	output	SPI clock output
sckz	output	SPI clock line tri-state buffer control

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic such as arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader loading new program into RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States, and allows core to work with different speed program memories.

External Memory Interface – Contains memory access related registers such as Data Pointer High (DPH0, DPH1), Data Pointer Low (DPL0, DPL1), Data Page Pointer (DPP0, DPP1), MOVX @Ri address register (MXAX) and STRETCH registers. It performs the memory addressing and data transfers. Allows applications software to access up to 16 MB of external data memory. The DPP0, DPP1 registers are used for segments swapping. STRETCH register allows flexible timing management while accessing different speed system devices by programming XRAMWR and XRAMRD pulse width between 1 – 8 clock periods.

Internal Data Memory Interface – Internal Data Memory interface controls access into the internal 256 bytes memory. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) using all direct addressing mode instructions.

http://www.DigitalCoreDesign.com
http://www.dcd.pl

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers such as Interrupt Enable (IE), Interrupt Priority (IP), Extended Interrupt Enable (EIE), Extended Interrupt priority (EIP) and (TCON) registers.

I/O Ports – Block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, P3.

Power Management Unit – Block contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode) to significantly reduce power consumption. Switchback feature allows UARTs, and interrupts to be processed in full speed mode if enabled. It is very desired when microcontroller is planned to use in portable and power critical applications.

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

Floating Point Unit – Block contains floating point arithmetic IEEE-754 compliant instructions (C *float, int, long int* types supported). It is used to execute single precision floating point operations such as: addition, subtraction, multiplication, division, square root, comparison absolute value of number and change of

sign. Basing on specialized CORDIC algorithm a full set of trigonometric operations are also allowed: sine, cosine, tangent, arctangent. It also has built-in integer to floating point and vice versa conversion instructions. FPU supports single precision real numbers, 16-bit and 32-bit signed integers. This unit has included standard software interface allows easy usage and interfacing with user C/ASM written programs.

Multiply Divide Unit – It's a fixed point fast 16-bit and 32-bit multiplication and division unit. It provides shift and normalize operations, additionally. All operations are performed using unsigned integer numbers. The MDU contains MD0 to MD5 operands, the result registers and one control register called ARCON. This unit has included standard software interface allows easy usage and interfacing with user C/ASM written programs.

Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 CLK periods when appropriate timer is enabled. In the counter mode the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

Timer 2 – Second system timer module contains one 16-bit configurable timer: Timer 2 (TH2, TL2), capture registers (RLDH, RLDL) and Timer 2 Mode (T2MOD) register. It can work as a 16-bit timer / counter, 16-bit auto-reload timer / counter. It also supports compare capture unit if it's presented in system. It can be used as clock source for UART0.

Compare Capture Unit – The compare / capture / reload unit is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing such as pulse generation, pulse width modulation, measurements etc.

Watchdog Timer – The watchdog timer is a 27-bit counter which is incremented every system clock periods (CLK pin). It performs system protection against software upsets.

UART0 – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning it can transmit and receive concurrently. Includes

Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2.

UART1 – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning it can transmit and receive concurrently. Includes Serial Configuration register (SCON1), serial receiver and transmitter buffer (SBUF1) registers. Its receiver is double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF1 loads the transmit register, and reading SBUF1 reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART1 is synchronized by Timer 1.

Master I2C Unit – I2C bus controller is a Master module. The core incorporates all features required by I2C specification. Supports both 7-bit and 10-bit addressing modes on the I2C bus. It works as a master transmitter and receiver. It can be programmed to operate with arbitration and clock synchronization to allow it operate in multi-master systems. Built-in timer allows operation from a wide range of the input frequencies. The timer allows to achieve any non-standard clock frequency. The I2C controller supports all transmission modes: Standard, Fast and High Speed up to 3400 kbs.

Slave I2C Unit – I2C bus controller is a Slave module. The core incorporates all features required by I2C specification. It works as a slave transmitter/receiver depending on working mode determined by a master device. The I2C controller supports all transmission modes: Standard, Fast and High Speed up to 3400 kbs.

SPI Unit – it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. SPI automatically drives slave select outputs SSO[7:0], and address SPI slave device to exchange serially shifted data. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

P E R F O R M A N C E

The following tables give a survey about the Core area and performance in Programmable Logic Devices after Place & Route (all key features have been included):

| Device	Speed grade	F_{max}
ACEX1K	-1	45 MHz
FLEX10KE	-1	46 MHz
APEX20KE	-1	48 MHz
APEX20KC	-7	57 MHz
APEX-II	-7	72 MHz
MERCURY	-5	92 MHz
STRATIX	-5	85 MHz
CYCLONE	-6	76 MHz

Core performance in ALTERA® devices

For a user the most important is application speed improvement. The most commonly used arithmetic functions and their improvements are shown in table below. An improvement was computed as {80C51 clock periods} divided by {DR8051XP clock periods} required to execute an identical function. More details are available in core documentation.

Function	Improvement
8-bit addition (*immediate data*)	7,20
8-bit addition (*direct addressing*)	6,00
8-bit addition (*indirect addressing*)	6,00
8-bit addition (*register addressing*)	7,20
8-bit subtraction (*immediate data*)	7,20
8-bit subtraction (*direct addressing*)	6,00
8-bit subtraction (*indirect addressing*)	6,00
8-bit subtraction (*register addressing*)	7,20
8-bit multiplication	9,60
8-bit division	8,73
16-bit addition	7,20
16-bit subtraction	7,64
16-bit multiplication	8,21
32-bit addition	7,20
32-bit subtraction	7,43
32-bit multiplication	7,70
Average speed improvement:	**7,28**

Dhrystone Benchmark Version 2.1 was used to measure Core performance. The following table gives a survey about the DR8051XP performance in terms of Dhrystone/sec and VAX MIPS rating.

Device	Target	Clock frequency	Dhry/sec (VAX MIPS)
80C51	-	12 MHz	268 (0.153)
80C310	-	33 MHz	1550 (0.882)
DR8051XP	MERCURY	90 MHz	16648 (9.450)

Core performance in terms of Dhrystones

Legend: ☐ 80C51 (12MHz) ☐ 80C310 (33MHz) ☐ DR8051XP (90MHz)
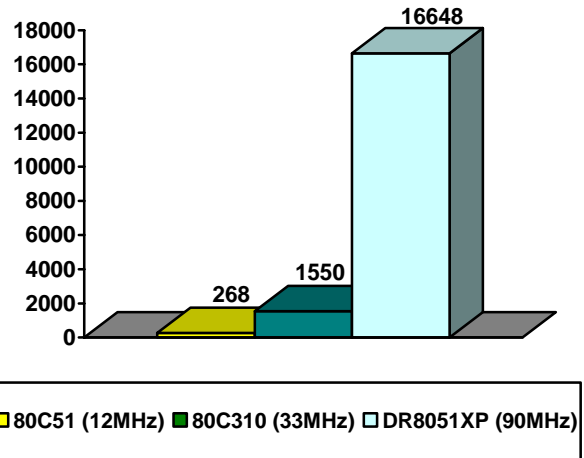
Area utilized by the each unit of DR8051XP core in vendor specific technologies is summarized in table below.

Component	Area [LC]	[FFs]
CPU*	1410	220
DPTR1 register	50	32
DPTR0 decrement	40	-
DPTR1 decrement	40	-
DPTR0 & DPTR1 auto-switch	30	8
Timed Access protection	20	10
Interrupt Controller	150	40
INT2-INT6	100	25
Power Management Unit	10	5
I/O ports	100	35
Timers	160	50
Timer 2	170	60
UART0	210	60
UART1	210	60
Master I2C Unit	260	120
Slave I2C Unit	160	70
SPI Unit	110	55
Compare Capture Unit	150	60
Watchdog Timer	100	45
Multiply Divide Unit	500	105
Total area	**3980**	**1060**

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

Core components area utilization

The main features of each DR8051XP family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space	Stack space size	Internal Data Memory space	External Data Memory space	External Data Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I/O Ports	Program Memory Wait States	Compare/Capture	Watchdog	Master I²C Bus Controller	Slave I²C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
DR8051CPU	6.7	64k	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-	-
DR8051	6.7	64k	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-	-
DR8051XP	6.7	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓	✓

DR8051 family of High Performance Microcontroller Cores

The main features of each DR80390 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space	Stack space size	Internal Data Memory space	External Data Memory space	External Data Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I/O Ports	Program Memory Wait States	Compare/Capture	Watchdog	Master I²C Bus Controller	Slave I²C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
DR80390CPU	6.7	16M	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-	-
DR80390	6.7	16M	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-	-
DR80390XP	6.7	16M	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓	✓

DR80390 family of High Performance Microcontroller Cores

CONTACTS

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php

http://www.DigitalCoreDesign.com
http://www.dcd.pl