# Precision Analog Microcontroller
# Cortex™-M3 with ISM band Transceiver

Preliminary Technical Data

# ADuCRF101

## FEATURES

**Analog I/O**
- 6-Channel 14-bit or 12-bit ADC
- Single ended and differential inputs
- Programmable data rate up to 842kSPS
- On-Chip Voltage Reference and Temperature Sensor

**Power**
- Supply Range: 2.2 V to 3.6 V
- Power Consumption
  - 680 nA, in power down mode, non-retained state
  - 1.6 µA, in power down mode, MCU memory and transceiver memory retained
  - 190 µA / MHz, Cortex in Active mode
  - 12.8 mA transceiver in receive mode, Cortex in power down mode
  - 9 to 32 mA transceiver in transmit mode, Cortex in power down mode

**RF Transceiver**
- Frequency bands
  - 862 MHz to 928 MHz
  - 431 MHz to 464 MHz
- Multiple Configurations supported
- Receiver sensitivity (BER)
  - -107.5 dBm at 38.4 kbps, 2FSK
- Single ended and differential PA
- Low External BOM

**Microcontroller**
- ARM Cortex™-M3 32-bit processor
- Serial Wire download and debug
- External Watch crystal for wakeup timer
- 16 MHz internal Oscillator with 8-way Programmable Divider

**Memory**
- 128k/64k Bytes Flash/EE Memory, 16k/8k Bytes SRAM
- 20000 cycle Flash/EE endurance
- 10 year Flash/EE retention
- In-circuit download via Serial Wire and UART

**On-Chip Peripherals**
- UART, I²C and SPI Serial I/O
- 28-Pin GPIO Port
- 2 General Purpose Timers
- Wake-up Timer
- Watchdog Timer
- 8-Channel PWM

**Packages and Temperature Range**
- 64 lead LFCSP (9mm x 9mm) package –40°C to 85°C

**Tools**
- Low-Cost Development System
- Third-Party Compiler and emulator tool Support

## APPLICATIONS

Battery powered wireless sensor
Medical telemetry systems
Industrial and home automation
Asset tracking
Security systems (access systems)
Health and fitness applications

## FUNCTIONAL BLOCK DIAGRAM

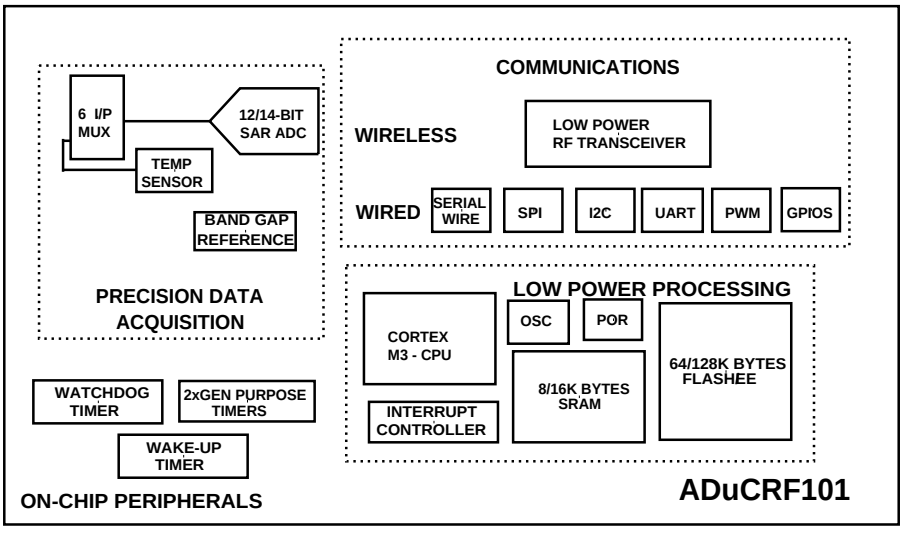


*Figure 1. ADuCF101 Block Diagram*

**Rev. PrF**


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# GENERAL DESCRIPTION

The ADuCRF101 is a fully integrated data acquisition solution designed for low power wireless applications. It features an 14-bit ADC, a low power Cortex™-M3 core from ARM®, a 431 MHz to 464 MHz and 862 MHz to 928 MHz RF transceiver, and Flash/EE memory packaged in a 9 mm × 9 mm LFCSP.

The acquisition section consists of a 14 bit SAR ADC. The six inputs can be configured as single ended or differential modes. When configured in single ended mode, they can be used for ratiometric measurements on sensors, powered when required from the internal LDO. An internal battery monitor channel and an on-chip temperature sensor are also available.

This wireless data acquisition system is designed to operate in battery-powered applications where low power is critical. The device can be configured in normal operating mode or different low power modes under direct program control. In flexi mode any peripheral can operate and wake-up the device. In hibernate mode the internal wake-up timer remains active. In shutdown mode only an external interrupt can wake-up the device.

The ADuCRF101 integrates a low power Cortex-M3 core from ARM. It is a 32-bit RISC machine, offering up to 1.25 DMIPS peak performance. The Cortex-M3 MCU also has a flexible 14-channel DMA controller supporting communication peripherals SPI, UART and I²C. 64 kB / 128 kB of nonvolatile Flash/EE memory and 8 kB /16 kB of SRAM are also provided on-chip.

A 16 MHz on-chip oscillator generates the system clock. This clock can be internally divided for the CPU to operate at lower frequency for power saving reasons. A low power internal 32 kHz oscillator is available and can used to clock the timers. There are two general-purpose timers, a wake-up timer and a system watchdog timer.

A range of communication peripherals can be configured as required in a specific application. These peripherals include UART, I²C, and SPI, GPIO ports, PWM and RF transceiver.

The RF transceiver communicates in the 431 MHz to 464 MHz and 862 MHz to 928 MHz frequency bands using multiple configurations.

On-chip factory firmware supports in-circuit serial download via the UART while nonintrusive emulation and program download is also supported via the serial wire interface. These features are incorporated into a low cost development system supporting this precision analog microcontroller family.

The parts operate from 2.2 V to 3.6 V and are specified over an industrial temperature range of −40°C to +85°C.

Three versions of the ADuCRF101 are available:

14-bit ADC, 128k Byte Flash and 16k Byte SRAM,

12-bit ADC, 128k Byte Flash and 16k Byte SRAM,

12-bit ADC, 64k Byte Flash and 8k Byte SRAM,

# SPECIFICATIONS

## ANALOG FRONT END SPECIFICATIONS

AVDD = IOVDD = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, $V_{REF}$ = 1.25 V internal reference, $f_{CORE}$ = 16 MHz, all specifications $T_A$ = $T_{MAX}$ to $T_{MIN}$, unless otherwise noted. Default ADC sampling frequency: eight acquisition clocks and ADC clock frequency of 4 MHz.

**Table 1. ADC channel specifications**

| | 12-bit model | | 14-bit model | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Typ** | **Max** | **Typ** | **Max** | **Unit** | **Test Conditions/Comments** |
| DC ACCURACY | | | | | | Single ended input mode. Applies to all ADC input channels. |
| Resolution | 12 | | 14 | | Bits | |
| Integral Nonlinearity | ±1 | | ±4 | | LSB | $V_{REF}$ = 1.25V from internal reference |
| | ±2 | | ±8 | | LSB | $V_{REF}$ = 1.8V from LDO |
| Differential Nonlinearity | ±1 | | ±1 | | LSB | Guaranteed no missing code |
| DC Code Distribution | 2 | | 8 | | LSB | ADC input is a DC voltage |
| CALIBRATED ENDPOINT ERRORS | | | | | | Measured using the factory-set default values ADCOF and ADCGN. |
| Offset Error | ±0.6 | | ±2.5 | | LSB | |
| Offset Error Match | ±0.25 | | ±1 | | LSB | |
| Gain Error | ±1.25 | | ±5 | | LSB | |
| Gain Error Match | ±0.25 | | ±1 | | LSB | |
| DYNAMIC PERFORMANCE | | | | | | $f_{IN}$ = 10 kHz sine wave. |
| Signal-to-Noise Ratio (SNR) | 68 | | 80 | | dB | |
| Total Harmonic Distortion | TBD | | TBD | | | |
| Peak Harmonic or Spurious Noise (PHSN) | TBD | | TBD | | | |
| Channel-to-Channel Crosstalk | TBD | | TBD | | | Measured on adjacent channels |

**Table 2. ADC channel specifications**

| **Parameter** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions/Comments** |
|---|---|---|---|---|---|
| ANALOG INPUT | | | | | |
| Input Voltage Ranges[1] | | | | | |
| Single ended input | 0 | | $V_{REF}$ | V | |
| Differential input | 0 | | $V_{CM} \pm V_{REF}/2$ | V | |
| Leakage Current | | 100 | | nA | |
| Input Capacitance | | 20 | | pF | During ADC Acquisition |
| ADC Power-up Time | | 5 | | µs | Excludes reference power up time |
| ON-CHIP VOLTAGE REFERENCE | | | | | |
| Output Voltage | | 1.25 | | V | |
| Accuracy | | ±5 | | mV | Measured at $T_A$ = 25°C |
| Reference Temperature Co | | ±40 | | ppm/°C | |
| Power Supply Rejection Ratio | | 60 | | dB | |
| Output Impedance | | 2 | | Ω | |
| Internal $V_{REF}$ Power-On Time | | 5 | | ms | 0.47µF external capacitor |
| TEMPERATURE SENSOR[1] | | | | | Indicates die temperature |
| Voltage Output at 25°C | | TBD | | mV | |
| Voltage TC | | TBD | | mV/°C | |
| Accuracy | | TBD | | °C | MCU in low power mode |
| Thermal impedance | | TBD | | | |

[1] These numbers are not production tested, but are guaranteed by design and/or characterization data at production release.

## CURRENT CONSUMPTION SPECIFICATIONS

AVDD = IOVDD = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, $f_{CORE}$ = 16 MHz, all specifications $T_A = T_{MAX}$ to $T_{MIN}$, unless otherwise noted.

**Table 3.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| CURRENT CONSUMPTION | | | | | |
| Cortex in SHUTDOWN mode | | 680 | | nA | RF transceiver in sleep mode, memory not retained |
| Cortex in HIBERNATE mode | | | | | Wake up timer running from external 32kHz crystal, 8kB of SRAM retained (8kB non-retained) |
| RF transceiver in sleep mode, memory retained | | 1.6 | | µA | |
| RF transceiver in sleep mode, memory not retained | | 1.38 | | µA | |
| RF transceiver in receive mode | | 12.8 | | mA | |
| RF transceiver in transmit mode | | 9 to 32 | | mA | |
| Cortex active, RF transceiver active | | | | | RF transceiver in PHY_ON or PHY_OFF state |
| Static current | | 1.8 | | mA | |
| Dynamic current | | 190 | | µA/MHz | |
| STARTUP TIME[1] | | | | | |
| Cortex at Power On | | 40 | | ms | |
| From SLEEP mode | | 3 to 5 | | FCLK | FCLK is the Cortex-M3 clock or divided version of the 16MHz oscillator. |
| Cortex from HIBERNATE mode | | 12 | | µs | |
| Cortex from SHUTDOWN mode | | 40 | | ms | |
| Transceiver from sleep mode | | 562.8 | | µs | Includes 310 µs for 26MHz crystal startup (7pF load capacitor at $T_A = 25^0C$) |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Power Supply Voltage Range[1] | 2.2 | | 3.6 | V | |

[1] These numbers are not production tested, but are guaranteed by design and/or characterization data at production release.

## RF LINK SPECIFICATIONS

AVDD = IOVDD = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted. RF frequency = 868 MHz.

**Table 4.**

| Parameter | Min | Typ | Max | Unit | Test Conditions / Comments |
|---|---|---|---|---|---|
| FREQUENCY RANGE | | | | | |
| | 862 | | 928 | MHz | |
| | 431 | | 464 | MHz | |
| PHASE-LOCKED LOOP | | | | | |
| Channel Frequency Resolution | | 396.7 | | Hz | |
| Phase Noise (In-Band) | | -88 | | dBc/Hz | 10 kHz offset, PA output power = 10 dBm |
| DATA RATE | | | | | |
| 2FSK | 1 | | 300 | kbps | |
| OOK | 2.4 | | 19.2 | kbps | Manchester Encoding enabled (Manchester chip rate = 2 x datarate) |
| Data rate resolution | | 100 | | bps | |
| TRANSMIT POWER RANGE[1] | | | | | |
| Single ended PA | | -20 to 13.5 | | dBm | Programmable. |
| Differential PA | | -20 to 10 | | dBm | Programmable. |
| MODULATION | | | | | |
| Deviation Frequency Resolution | | 100 | | Hz | |
| 2FSK/GFSK INPUT SENSITIVITY, BIT ERROR RATE (BER) | | | | | At BER = $10^{-3}$ |
| 1.0 kbps | | -116 | | dBm | Frequency deviation = 10 kHz, IF filter bandwidth = 100 kHz |
| 38.4 kbps | | -107.5 | | dBm | Frequency deviation = 19.2 kHz, IF filter bandwidth = 100 kHz |
| 300 kbps | | -100.5 | | dBm | Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz |
| 2FSK/GFSK INPUT SENSITIVITY, PACKET ERROR RATE (PER) | | | | | At PER = 1%, packet length =20 bytes, packet mode |
| 1.0 kbps | | -115.5 | | dBm | Frequency deviation = 10 kHz, IF filter bandwidth = 100 kHz |
| 38.4 kbps | | -106 | | dBm | Frequency deviation = 19.2 kHz, IF filter bandwidth = 100 kHz |
| 300 kbps | | -98 | | dBm | Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz |
| ADJACENT CHANNEL REJECTION | | | | | |
| CW Interferer | | | | | Wanted signal 3 dB above the input sensitivity level (BER = $10^{-3}$), CW interferer power level increased until BER = $10^{-3}$, image calibrated |
| 200 kHz Channel Spacing | | 38 | | dB | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = 12.5 kHz, DR = 50 kbps |
| 300 kHz Channel Spacing | | 39 | | dB | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = 25 kHz, DR = 100 kbps |
| 300 kHz Channel Spacing | | 38 | | dB | IF BW = 150 kHz, wanted signal: $F_{DEV}$ = 37.5 kHz, DR = 150 kbps |
| 400 kHz Channel Spacing | | 40 | | dB | IF BW = 200 kHz, wanted signal: $F_{DEV}$ = 50 kHz, DR = 200 kbps |
| 600 kHz Channel Spacing | | 41 | | dB | IF BW = 300 kHz, wanted signal: $F_{DEV}$ = 75 kHz, DR = 300 kbps |

| | | | |
|---|---|---|---|
| Modulated Interferer | | | Wanted signal 3 dB above the input sensitivity level (BER = $10^{-3}$), modulated interferer with the same modulation as the wanted signal; interferer power level increased until BER = $10^{-3}$, image calibrated |
| 200 kHz Channel Spacing | 38 | dB | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = 12.5 kHz, DR = 50 kbps |
| 300 kHz Channel Spacing | 36 | dB | IF BW = 100 kHz, wanted signal: $F_{DEV}$ = 25 kHz, DR = 100 kbps |
| 300 kHz Channel Spacing | 36 | dB | IF BW = 150 kHz, wanted signal: $F_{DEV}$ = 37.5 kHz, DR = 150 kbps |
| 400 kHz Channel Spacing | 34 | dB | IF BW = 200 kHz, wanted signal: $F_{DEV}$ = 50 kHz, DR = 200 kbps |
| 600 kHz Channel Spacing | 35 | dB | IF BW = 300 kHz, wanted signal: $F_{DEV}$ = 75 kHz, DR = 300 kbps |
| CO-CHANNEL REJECTION | -4 | dB | Desired signal 10 dB above the input sensitivity level (BER = $10^{-3}$), data rate = 38.4 kbps, frequency deviation = 20 kHz. |
| BLOCKING, ETSI EN 300 220 | | | Measurement procedure as per ETSI EN 300 220-1 V2.3.1; desired signal 3 dB above the ETSI EN 300 220 reference sensitivity level of −99 dBm, IF bandwidth =100 kHz, data rate = 38.4 kbps, unmodulated interferer. |
| ±2 MHz | -28 | dBm | |
| ±10 MHz | -20.5 | dBm | |
| WIDEBAND INTERFERENCE REJECTION | 75 | dB | Swept from 10 MHz to 100 MHz either side of the RF frequency |
| IMAGE CHANNEL ATTENUATION | | | Measured as image attenuation at the IF filter output, carrier wave interferer at 400 kHz below the channel frequency, 100 kHz IF filter bandwidth |
| 868 MHz | 36/45 | dB | Uncalibrated[2]/calibrated |

[1] Measured as the maximum unmodulated power.
[2] Measured with IMAGE_REJECT_CAL_AMPLITUDE = 0x7 and IMAGE_REJECT_CAL_PHASE = 0x16.

## GENERAL ELECTRICAL SPECIFICATIONS

AVDD = IOVDD = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, $V_{REF}$ = 1.25V internal reference, $f_{CORE}$ = 16 MHz, all specifications $T_A$ = $T_{MAX}$ to $T_{MIN}$, unless otherwise noted.

**Table 5.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| POWER SUPPLY MONITOR | | | | | |
| Trip Point voltage | | 2 | | V | |
| Trip Point accuracy | | 2 | | % | |
| POWER-ON-RESET | | 1.67 | | V | |
| Watchdog Timer[1] | | | | | |
| Timeout Period | 0 | | 512 | s | Programmable |
| Flash/EE MEMORY[1] | | | | | |
| Endurance[2] | 20,000 | | | Cycles | |
| Data Retention[3] | 10 | | | Years | $T_J$ = 85°C |
| Digital Inputs | | | | | All digital inputs, excluding LFXTAL1 and XOSC26P |
| Input Current (leakage current) | | 10 | | nA | $V_{INH}$ = IOVDD or $V_{INH}$ = 2.2V, pull up disabled. $V_{INL}$ = 0V, pull up disabled. |
| Input Capacitance | | 10 | | pF | |
| Logic Inputs | | | | | All Logic inputs, including LFXTAL1, excluding XOSC26P |
| VINL, Input Low Voltage | | | 0.2 x IOVDD | V | |
| VINH, Input High Voltage | 0.7 x IOVDD | | | V | |
| Logic Outputs | | | | | |
| VOH, Output High Voltage | IOVDD – 0.4 | | | V | $I_{source}$ = 1mA |
| VOL, Output Low Voltage | | | 0.36 | V | $I_{sink}$ = 1mA |
| 32.768kHz CRYSTAL | | | | | 32.768 kHz crystal, for use with timers and/or RF transceiver wake up controller. |
| Input Current (leakage current) | | 50 | | nA | $V_{INH}$ = IOVDD or $V_{INH}$ = 2.2V. $V_{INL}$ = 0V. |
| LFXTAL1 Input Capacitance | | 2 | | pF | |
| LFXTAL2 Output Capacitance | | 2 | | pF | |
| 26MHz CRYSTAL | | | | | |
| XOSC26P Input Capacitance | | 10 | | pF | |
| XOSC26N Output Capacitance | | 10 | | pF | |
| INTERNAL HF OSCILLATOR | | 16 | | MHz | MCU clock by default |
| Tolerance | | ±3 | | % | |
| INTERNAL LF OSCILLATOR | | 32.768 | | kHz | |
| Tolerance | | ±20 | | % | |
| MCU CLOCK DIVIDER[1] | 1 | | 128 | | 8 programmable core clock dividers. |
| EXTERNAL CLOCK INPUT[1] | | | | | External MCU clock range allowed |
| Range | 32.768 | | 16000 | kHz | |

[1] These numbers are not production tested, but are guaranteed by design and/or characterization data at production release.
[2] Endurance is qualified to 20,000 cycles as per JEDEC Std. 22 Method A117 and measured at –40°C, +25°C, and +85°C. Typical endurance at 25°C is 170,000 cycles.
[3] Retention lifetime equivalent at a junction temperature ($T_J$) of 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise noted

**Table 6.**

| Parameter | Rating |
|---|---|
| AVDD, IOVDD, VDDBAT1 and VDDBAT2 to GND | −0.3 V to 3.96V |
| Digital Input Voltage to GND | −0.3 V to 3.96V |
| Digital Output Voltage to GND | −0.3 V to 3.96V |
| $V_{REF}$ to GROUND | −0.3 V to 3.96V |
| Analog Inputs to GND | −0.3 V to 2.1V |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature | 105°C |
| $\theta_{JA}$ Thermal Impedance | |
| 64-Pin LFCSP _VQ | 25°C/W |
| Peak Solder Reflow Temperature | |
| Pb-Free Assemblies (30 s) | 260°C |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

The exposed paddle of the LFCSP package should be connected to ground.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

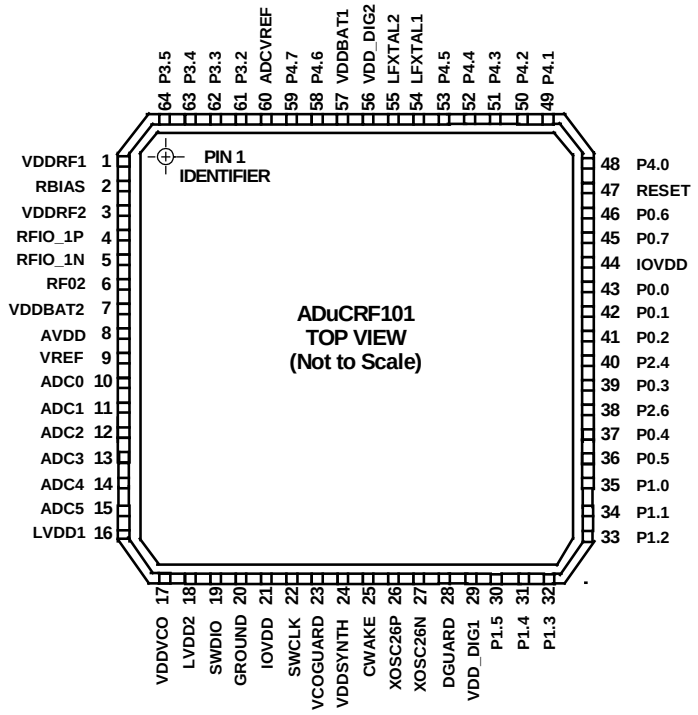


*Figure 8. 64-Lead LFCSP_VQ Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | VDDRF1 | Voltage Regulator output for RF circuits. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 2 | RBIAS | External bias resistor. A 36 kΩ resistor with 2% tolerance should be used. |
| 3 | VDDRF2 | Voltage Regulator output for RF block. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 4 | RFIO_1P | LNA Positive Input in Receive Mode. Differential PA Positive Output in Transmit Mode. |
| 5 | RFIO_1N | LNA Negative Input in Receive Mode. Differential PA Negative Output in Transmit Mode. |
| 6 | RF02 | Single ended PA output. |
| 7 | VDDVBAT2 | Battery Terminal, supply for the LDOs used in the RF section of the transceiver. |
| 8 | AVDD | Battery terminal, Supply for analog circuits such as ADC and ADC internal reference, POR, PSM and LDOs. |
| 9 | VREF | Internal 1.25V ADC reference. A 0.47 µF capacitor between this pin and ground is required. |
| 10 | ADC0 | ADC input channel 0 |
| 11 | ADC1 | ADC input channel 1 |
| 12 | ADC2 | ADC input channel 2 |
| 13 | ADC3 | ADC input channel 3 |
| 14 | ADC4 | ADC input channel 4 |
| 15 | ADC5 | ADC input channel 5 |
| 16 | LVDD1 | On chip LDO decoupling output. Connect a 0.47 µF capacitor to the 1.8V output to ensure core operating voltage is stable. |
| 17 | VDDVCO | Voltage Regulator output for VCO. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 18 | LVDD2 | On chip LDO decoupling output. Connect a 0.47 µF capacitor to the 1.32V output to ensure core operating voltage is stable |
| 19 | SWDIO | Serial Wire bi-directional data |
| 20 | GND | Ground pin, should be connected to the PADDLE. |
| 21 | IOVDD | Battery terminal, General Purpose IO supply. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 22 | SWCLK | Serial Wire debug clock |
| 23 | VCOGUARD | Guard, screen for VCO, should be connected to VDDVCO. |
| 24 | VDDSYNTH | Voltage Regulator output for Synthesizer. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 25 | CWAKE | External capacitor for wake up control. A 150 nF capacitor should be placed between this pin and ground. |
| 26 | XOSC26P | The 26MHz reference crystal should be connected between this pin and XOSC26N. |
| 27 | XOSC26N | The 26MHz reference crystal should be connected between this pin and XOSC26P. |
| 28 | DGUARD | Internal Guard, Screen for Digital Cells, should be connected to VDD_DIG1. |
| 29 | VDD_DIG 1 | Voltage Regulator output for Digital. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 30 | P1.5/IRQ6/I2CSDA/PWM7 | General Purpose Input and Output Port 1.5/External Interrupt 6/I2C Serial Data/PWM channel 7. |
| 31 | P1.4/IRQ5/I2CSCL/PWM6 | General Purpose Input and Output Port 1.4/External Interrupt 5/I2C Serial Clock/PWM channel 6. |
| 32 | P1.3/PWM5 | General Purpose Input and Output Port 1.3/PWM channel 5. |
| 33 | P1.2/PWM4 | General Purpose Input and Output Port 1.2/PWM channel 4. |
| 34 | P1.1/PORB/ TXD /PWM3 | General Purpose Input and Output Port 1.1/POR output/ UART TXD/ PWM channel 3. |
| 35 | P1.0/RXD/IRQ4/ MOSI /PWM2 | General Purpose Input and Output Port 1.0/UART RXD/ External Interrupt 4/ SPI1 Master Out Slave In Pin (MOSI)/PWM channel 2. |
| 36 | P0.5/$\overline{CS2}$ /ECLKIN | General Purpose Input and Output Port 0.5/SPI1 Chip Select 2/External Clock Input |
| 37 | P0.4/$\overline{CS1}$ /ECLKOUT | General Purpose Input and Output Port 0.4/SPI1 Chip Select 1/External Clock Output. |
| 38 | P2.6/GP0 | General Purpose Input and Output Port 2.6 |
| 39 | P0.3/IRQ1/$\overline{CS0}$ /ADCCONVST/PWM1 | General Purpose Input and Output Port 0.3/External Interrupt 1/SPI1 Chip Select 0/ADC convert start/PWM channel 1. |
| 40 | P2.4/IRQ8 | General Purpose Input and Output Port 2.4/ External Interrupt 8 |
| 41 | P0.2/MOSI/PWM 0 | General Purpose Input and Output Port 0.2/SPI1 Master Out Slave In Pin (MOSI)/PWM channel 0. |
| 42 | P0.1/SCLK | General Purpose Input and Output Port 0.1/SPI1 Serial Clock |
| 43 | P0.0/MISO | General Purpose Input and Output Port 0.0/SPI1 Master In Slave Out Pin (MISO) |
| 44 | IOVDD | General Purpose I/O supply. Connect to the battery terminal |
| 45 | P0.7/IRQ3/$\overline{CS4}$ /CTS | General Purpose Input and Output Port 0.7/ External Interrupt 3 / SPI1 Chip Select 4/ UART hand shake. |
| 46 | P0.6, $\overline{BOOT}$/ IRQ2/$\overline{CS3}$ / RTS/PWM0 | General Purpose Input and Output Port 0.6, BOOT pin / External Interrupt 2/ SPI1 Chip Select 3 / UART hand shake/PWM channel 0. |
| 47 | RESET | Active Low. A low signal on this pin for 24 system clocks will cause the part to reset. |
| 48 | P4.0/PWM0 | General Purpose Input and Output Port 4.0/PWM channel 0. |
| 49 | P4.1/PWM1 | General Purpose Input and Output Port 4.1/PWM channel 1. |
| 50 | P4.2/PWM2 | General Purpose Input and Output Port 4.2/PWM channel 2. |
| 51 | P4.3/PWM3 | General Purpose Input and Output Port 4.3/PWM channel 3. |
| 52 | P4.4/PWM4 | General Purpose Input and Output Port 4.4/PWM channel 4. |
| 53 | P4.5/PWM5 | General Purpose Input and Output Port 4.5/PWM channel 5. |
| 54 | LFXTAL1 | 32.768kHz watch crystal output for WU timers. |
| 55 | LFXTAL2 | 32.768kHz watch crystal input for WU timers. |
| 56 | VDD_DIG2 | Voltage Regulator output for Digital section of the transceiver. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. |
| 57 | VDDBAT1 | Battery Terminal, supply for the digital section of the transceiver and GPIOs. |
| 58 | P4.6/PWM6 | General Purpose Input and Output Port 4.6/PWM channel 6. |
| 59 | P4.7/PWM7 | General Purpose Input and Output Port 4.7/PWM channel 7. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 60 | ADCVREF | Transceiver's ADC Reference Output. A 220 nF capacitor should be placed between this pin and ground for adequate noise rejection. |
| 61 | P3.2/PWMSYNC | General Purpose Input and Output Port 3.2/PWM synchronisation. |
| 62 | P3.3/PWMTRIP | General Purpose Input and Output Port 3.3/PWM safety cut off. |
| 63 | P3.4 | General Purpose Input and Output Port 3.4. |
| 64 | P3.5 | General Purpose Input and Output Port 3.5. |
| 65 | PADDLE | The exposed package paddle should be soldered to a metal pad on the PCB, and connected to ground. |

# OUTLINE DIMENSIONS

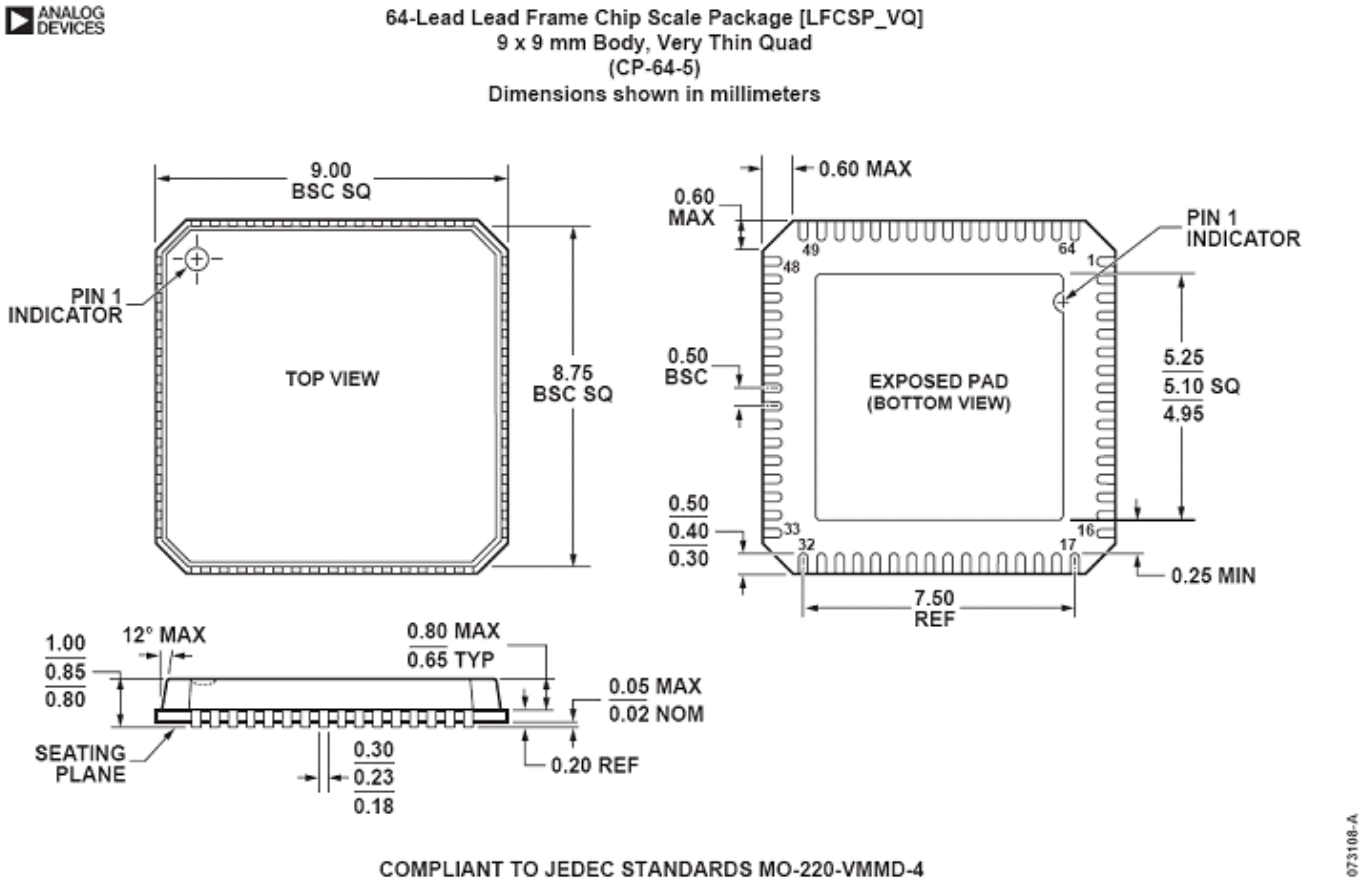


*Figure 2. 64-Lead Frame Chip Scale Package [LFCSP_VQ]*
*9 mm x 9 mm Body, Very Thin Quad*
*(CP-64-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Description | Package Option |
|---|---|---|---|
| | -40°C to 85°C | 14-bit ADC, 128k Byte Flash and 16k Byte SRAM | 64-lead LFCSP |
| | -40°C to 85°C | 12-bit ADC, 128k Byte Flash and 16k Byte SRAM | 64-lead LFCSP |
| | -40°C to 85°C | 12-bit ADC, 64k Byte Flash and 8k Byte SRAM | 64-lead LFCSP |
| | -40°C to 85°C | Evaluation board for 433MHz operation | n/a |
| | -40°C to 85°C | Evaluation board for 868/915MHz operation | n/a |

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


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