LCD Multimedia HSMC

Reference Manual

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Document Date: August 2008

Part Number MNL-01028-1

Contents

1. Overview

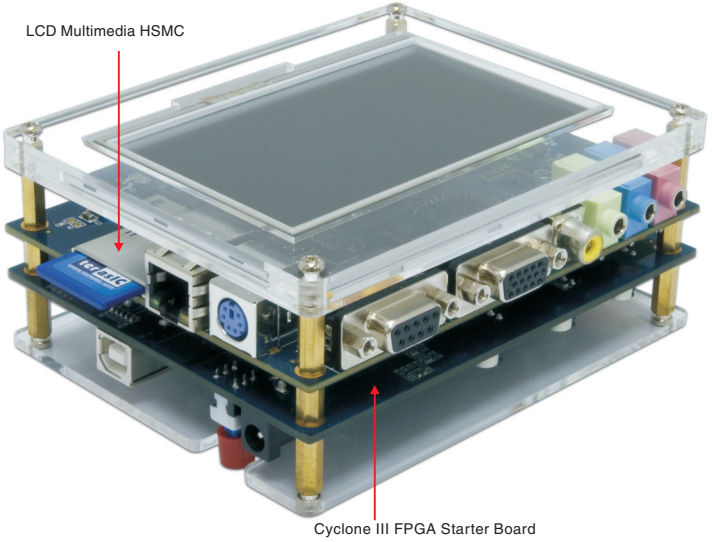
General Description

This manual provides comprehensive information about the LCD Multimedia High Speed Mezzanine Card (HSMC). This HSMC is a full-featured multimedia board that can be used for video, audio, and ethernet applications with many of the Altera FPGA Starter and Development boards that support the HSMC connectors. For example, see Figures 1–1.

The LCD Multimedia HSMC was created to provide a set of interfaces including LCD touchscreen, VGA out, composite video in, audio in/out, microphone in, plus Ethernet, SD-Card, PS/2, and RS-232 interfaces. The purpose of this reference manual is to describe each of these hardware interfaces on the LCD HSMC.

For the latest information about available HSMC boards, go to **www.altera.com/products/devkits/kit-index.html**.

Figure 1–1. LCD Multimedia HSMC in Nios II Embedded Evaluation Kit

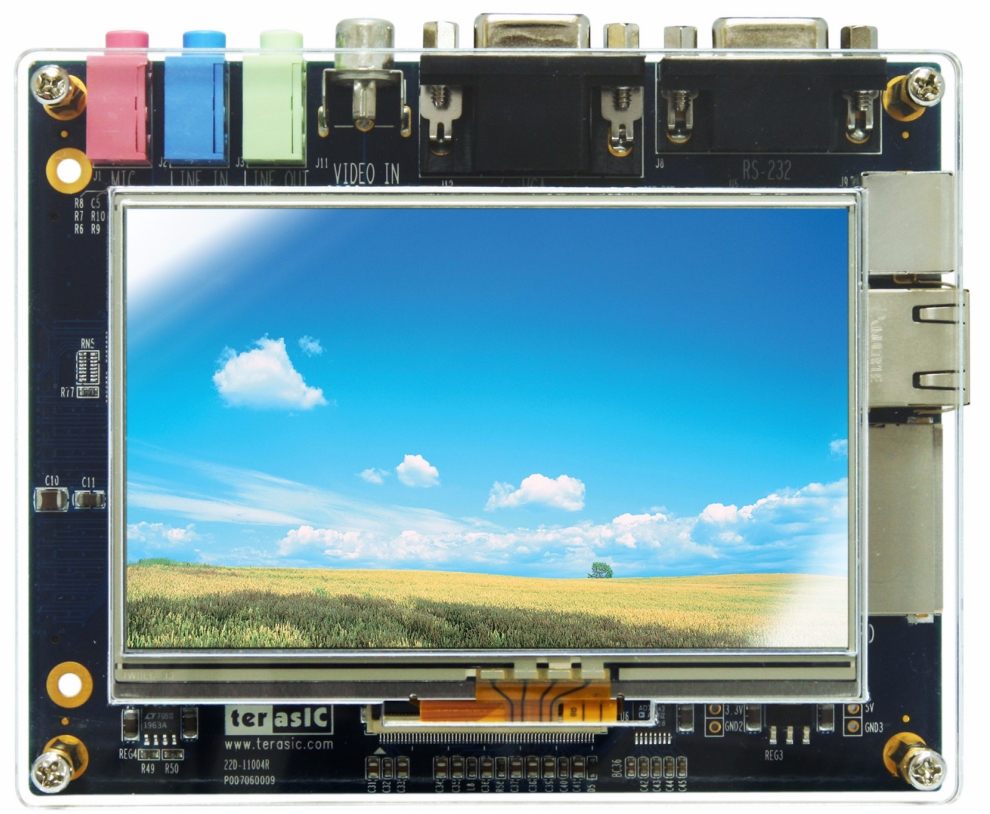


The top view of the LCD Multimedia HSMC is shown in Figure 1–2.

There are several sample software applications that highlight the LCD Touchpanel, SD-Card, and Ethernet components of the LCD Multimedia HSMC in the Nios II Development Kits.

For more information, refer *Nios II Embedded Evaluation kit Getting Started User Guide* as an example.

Figure 1–2. Top View of the LCD Multimedia HSMC



Connector view1 and connector view2 of the LCD Multimedia HSMC is shown in Figure 1–3 and Figure 1–4.

Figure 1–3. LCD Multimedia HSMC Side View 1

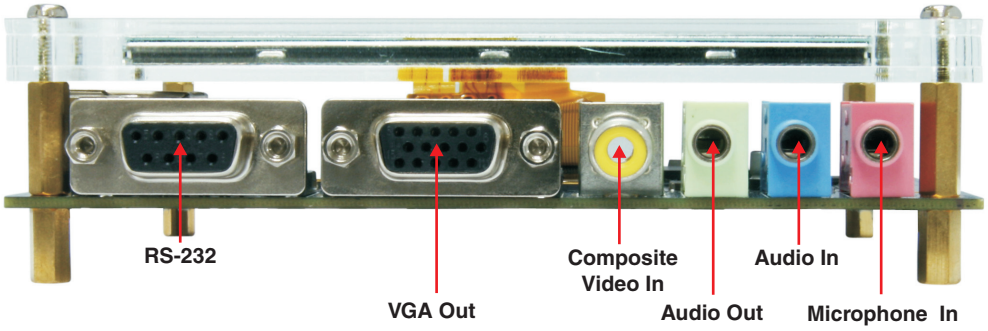
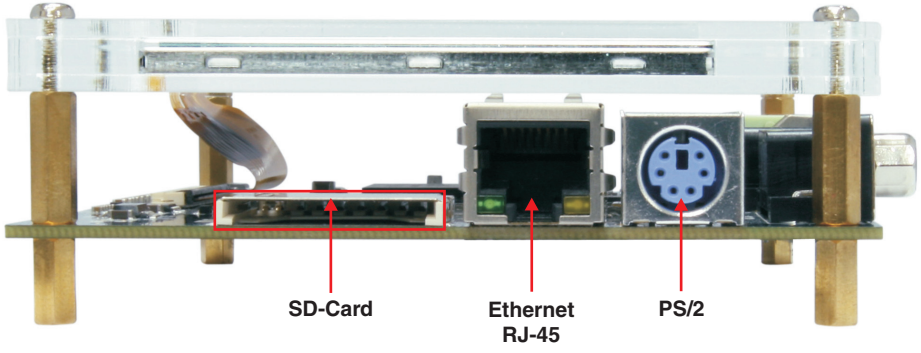


Figure 1–4. LCD Multimedia HSMC Side View 2



Components and Block Diagram

The LCD Multimedia HSMC contains the following components.

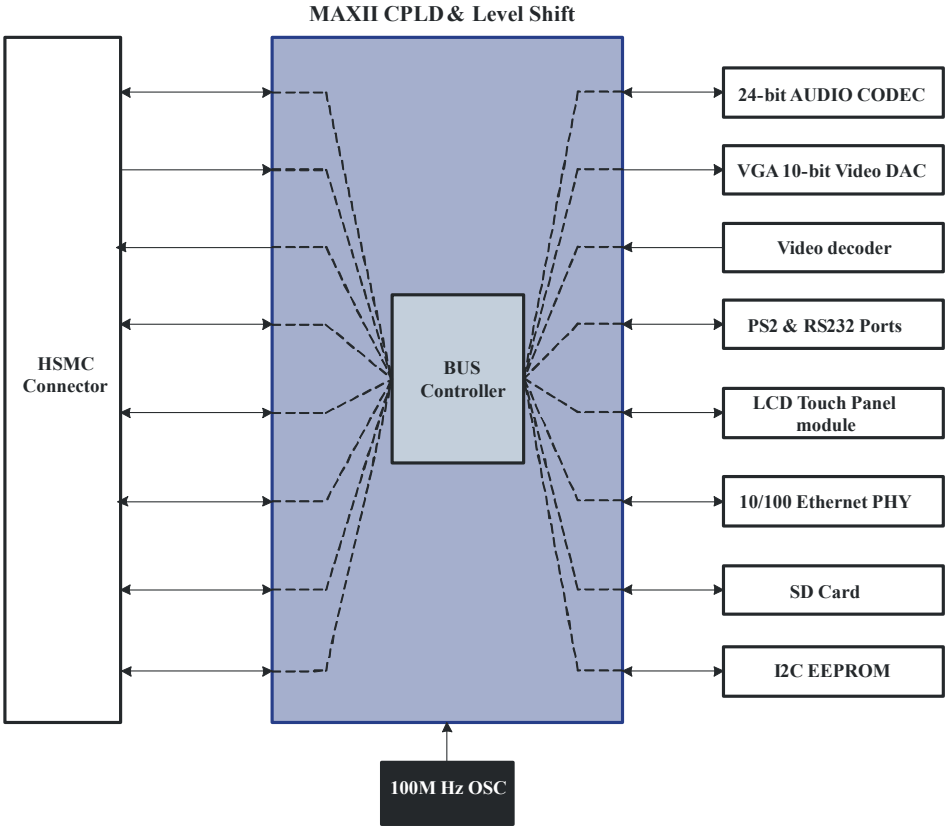
- MAX II CPLD EPM2210F324
  - 2210 Logic elements
  - 272 User I/Os
  - 324 pin FineLine BGA package
- LCD Touch-screen Display
  - 800 X 480 pixel 4.3" Display

- 24-bit Audio Codec
- SD Flash Connector
- 10/100 Ethernet physical layer (PHY)
- PS/2 Connector
- Other Interfaces
  - RS-232 Level-shifters
  - RCA Jack (Video In)
  - 10-bit VGA Output DAC
  - Composite Video ADC

Block Diagram

Figure 1–5 shows a functional block diagram of the LCD Multimedia HSMC.

Figure 1–5. LCD Multimedia HSMC



2. Board Components and Interfaces

Board Overview

This chapter provides operational and connectivity detail for the LCD Multimedia HSMC's major components and interfaces and is divided into the following major blocks:

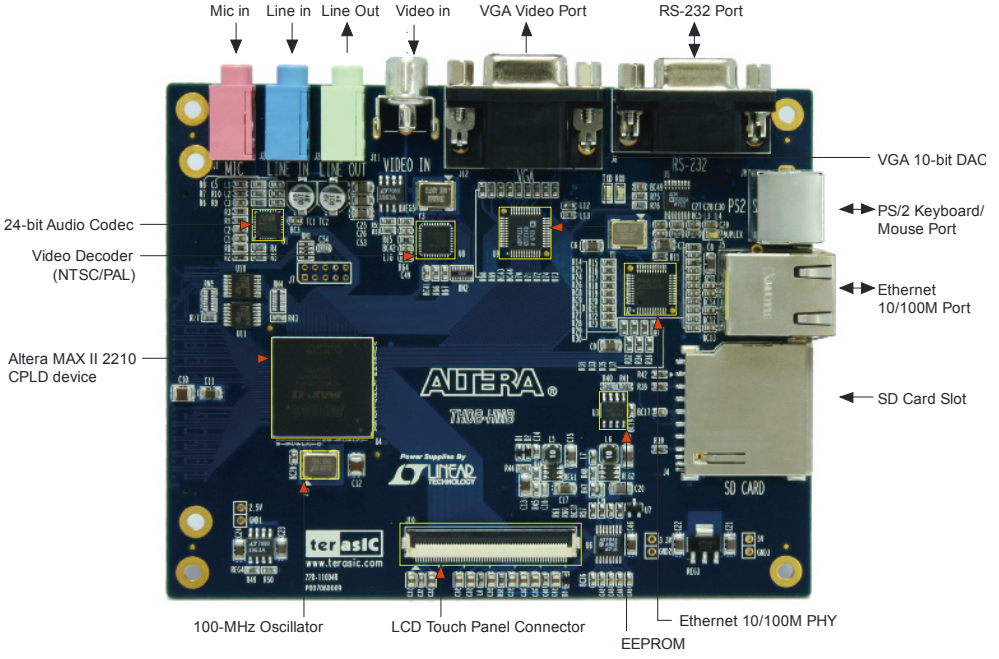
- MAX II CPLD used for
  - Time-division multiplexing of signals
  - Voltage level shifting
- Interfaces
  - HSMC expansion interface
  - Audio codec interface
  - Video decoder interface
  - VGA interface
  - Serial interface
  - PS/2 interface
  - Ethernet
- Clocking circuitry
- Memory
- Power supply

Board schematics, board layout database, and assembly files for the LCD Multimedia HSMC are included in the board_design_files subdirectory of the installed kit directory.

For information on powering-up the LCD Multimedia HSMC and installing the demo software and examples, refer to the user guide provided with your kit.

Figure 2–1 shows the top view of the LCD Multimedia HSMC.

Figure 2–1. Top View of the LCD Multimedia HSMC



Notes:
(1) LCD Touch Panel is not shown.

Figure 2–2 shows the back view of the LCD Multimedia HSMC.

Figure 2–2. Back View of the LCD Multimedia HSMC

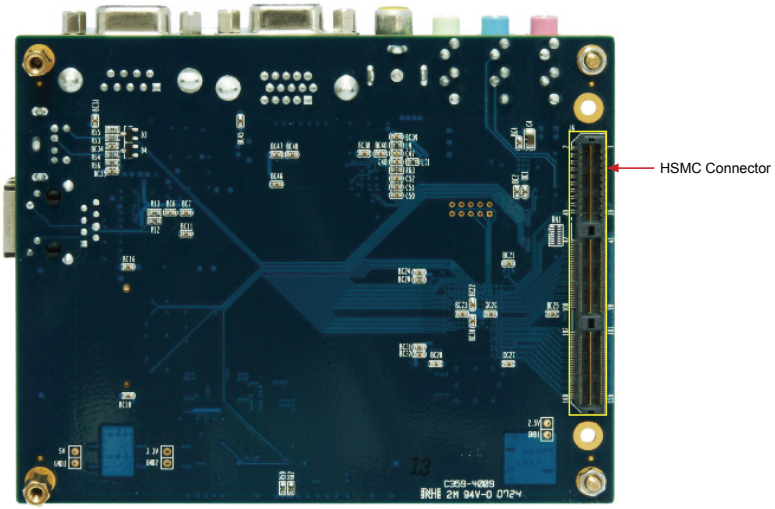


Table 2–1 lists the components and their corresponding board references.

Table 2–1. LCD Multimedia HSMC (Part 1 of 2)

Type	Component/ Interface	Board Reference	Description	Page
Interface Device				
CPLD	MAX II	U4	EPM2210F324C4, 272-pin FineLine BGA 324-pin package	2–4
Level Translator				
I/O	Bidirectional Level Shift Interface	U10, U11	MAX 3378 Dual Low-Voltage Level Translators	2–8
Display				
I/O	LCD Touch Screen Display	J10 +Touchscreen, U6	FPC 60B connector	2–10
Connections & Interfaces				
Input	MIC In	J1, U1	Microphone in jack	2–15

Table 2–1. LCD Multimedia HSMC (Part 2 of 2)

Type	Component/ Interface	Board Reference	Description	Page
Input	Line In	J2, U1	24 bit CD quality audio CODEC	2–15
Output	Line Out	J3, U1	24 bit CD quality audio CODEC	2–15
Input	SD Card Socket	J4	128 MB Memory Card	2–17
I/O	Ethernet	J5, U2	10/100 Ethernet PHY/MAC controller	2–19
I/O	RS 232	J8, U5	9 pin connector and transceiver	2–21
I/O	PS/2	J9	5 pin connector, mouse/ keyboard connector	2–22
Input	Video Decoder	J11	RCA jack	2–23
Output	VGA	J12, U9	One VGA output connector (DB15), and 10-bit VGA DAC	2–26
Clock Circuitry				
Oscillator	Clock	Y1, Y2, Y3	Various clock oscillators used for system clock or other dedicated devices.	2–30
Power Supply				
Power Supplies	Analog/Digital Power	Reg1, Reg2, Reg3, Reg4, Reg5	Switching and linear regulators used for powering analog and digital components.	2–31
EEPROM				
Memory	I2C EEPROM	U3	Uses one 2K bit EEPROM.	2–32
Expansion Interface				
I/O	HSMC	J6	Expansion connector used to interface with Altera starter and development boards	2–34

Interface Device

MAX II CPLD-EPM2210F324 (U4)

The LCD Multimedia HSMC uses the MAX II 2210 CPLD EPM2210F324C3 device (U4). Table 2–2 lists MAX II CPLD board reference and manufacturing information.

Table 2–2. MAX II CPLD Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U4	MAX II CPLD for TDM and level shifting/buffering	Altera	EPM2210F324C3N	www.altera.com

The primary functions for this device are to

1. Provide time-division multiplexing (TDM) functions to the LCD and VGA color data bus.

2. Provide level shifting feature for the 2.5V input (Cyclone III FPGA) and 3.3V required by many of the interface chips.

This package has 272 user I/Os and comes in a 324-pin Fine-Line BGA package. Table 2–3 lists Max II device features.

Table 2–3. Max II Device Features

Architectural Feature	Results
Altera's second generation low-cost CPLDs	• Low cost packaging • Large number of logic elements • LUT based architecture • Fastest CPLD supports up to 300MHz clock frequency
Lowest power consumption CPLD	• Power down capability that conserves the battery life • Lowest dynamic power • Hot-socketing support • Single power supply simplicity
On-chip user Flash memory	• 8kbit user accessible flash memory • Enables the integration of discrete and non-volatile storage reducing chip count and cost
Real time In-signal programmability	• Capable of downloading a second design while the device is operational
I/O capabilities	• Supports interfacing with 1.8V, 2.5V and 3.3V logic levels of the device due to Multivolt I/O capability • Schmitt triggers, programmable slew rate & programmable drive strength improve signal integrity

Table 2–4 lists the Max II EPM2210F324C4 device pin count.

Table 2–4. Max II Device Pin Count

Board Component	Pins
SD Card	6
Ethernet	18
Audio Codec	6
RS232 and PS/2	4
LCD Touch Panel	38
Video Decoder	14
VGA	25
MAX II CPLD ISP	4
HSMC(1)	88
Total Pins Used	203
Total EPM2210F324C4 User I/Os	272
Unused pins	69

Note to Table 2–4:
(1) The HSMC pins include all pins between the FPGA and the MAX II CPLD

For additional information about Altera devices, go to **www.altera.com/products/devices**.

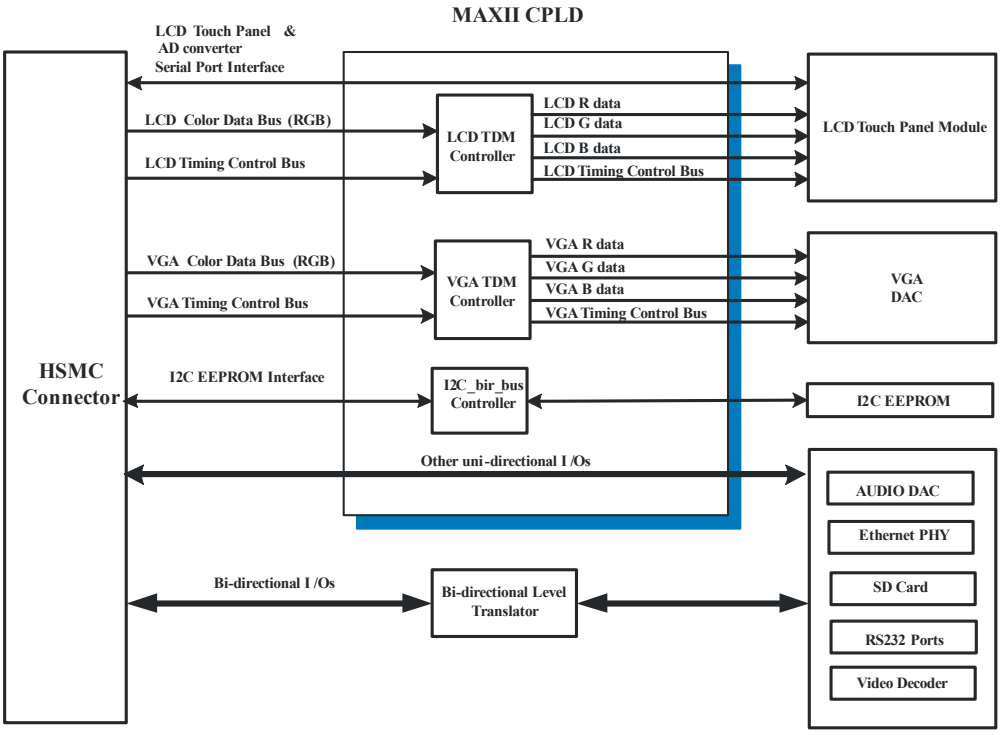
Block Diagram of bus-controller logic in the MAX II CPLD

Figures 2–3 shows the block diagram of Bus Controller logic in the MAX II device. Both the LCD TDM block is a simple 8-bit to 24-bit data de-multiplexing function which drives the LCD panel. Similarly, the VGA TDM block is a 10bit to 30bit data de-multiplexing function which drives the VGA DAC. In the LCD TDM block, the 8-bit input data (successive BGR color data) comes in at 3x the rate of the 24-bit output data bus (8-bit B + 8bit G + 8bit R).

The purpose of adding this complexity to the design of the LCD Multimedia HSMC was to allow for more functionality given the constraint of a pin-limited HSMC connector interface.

The I2CBir_bus block provides birdirectional control for I2C Serial EEPROM data bus. All other signals that pass through the MAXII device are uni-directional and are simply buffered and level-shifted in the MAX II.

Figure 2–3. The Block Diagram of MAX II Bus Controller



The source code for this design in the MAXII device can be found in the *"board_design_files"* directory for your development kit.

Level Translator

Bidirectional level shift interface

The board provides bidirectional level shift feature for the 2.5V input (Cyclone III FPGA) and 3.3V required by many of the interface chips via two Maxim MAX3378 level translators. Table 2–5 lists bidirectional level shift interface reference and manufacturing information.

Table 2–5. Bidirectional Level Shift Interface Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U10, U11	Dual Low-Voltage Level Translators	Maxim Integrated Products	MAX3378EEUD	www.maxim-ic.com

Figure 2–4 shows the block diagram and pinout of the bidirectional level shift interface on the board respectively.

Figure 2–4. Block Diagram of Bidirectional Level Shift Interface

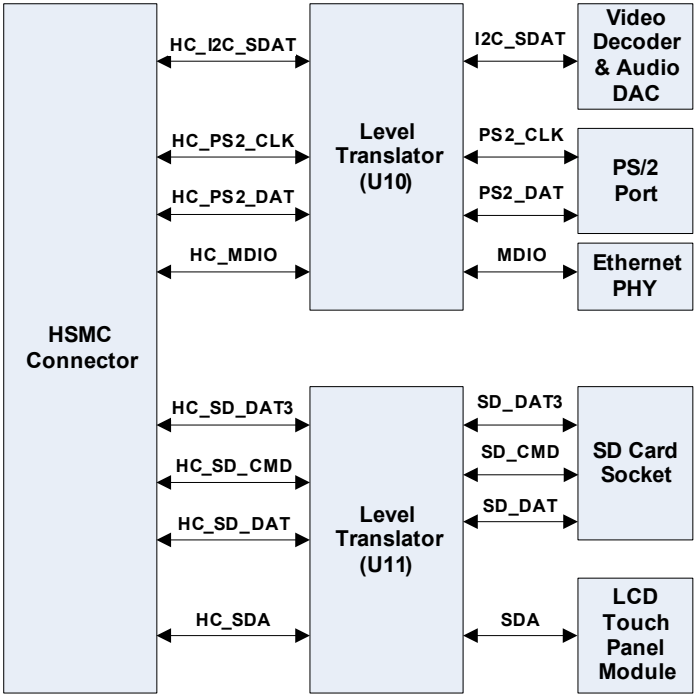


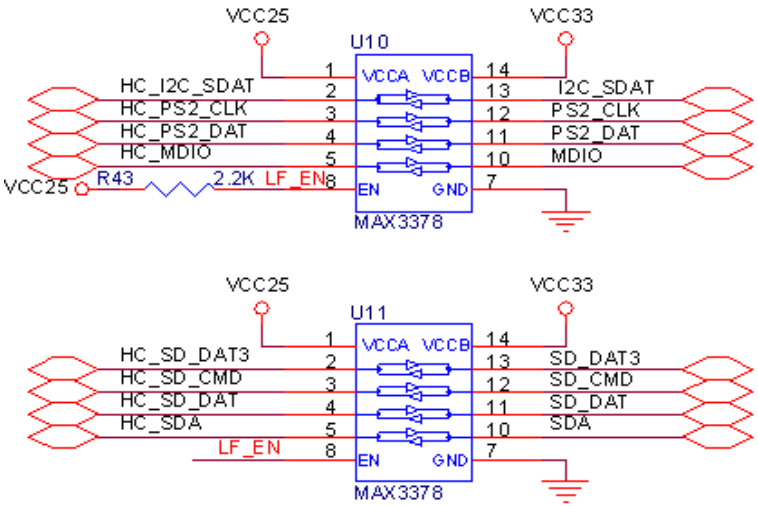
Table 2–6 shows the pinouts of Level Shift Inteface with HSMC connector.

Table 2–6. Level Shift Interface Pinouts with HSMC Connector

HSMC Side Signal Name	HSMC Pin No.	Device Side Signal	Level Shift Interface Pin No.	Level Shift Interface Description
HC_I2C_SDAT	33	I2C_SDAT	U1-27;U8-33	Audio CODEC ADC LR Clock
HC_PS2_CLK	43	PS2_CLK	J9-6	PS/2 Clock
HC_PS2_DAT	47	PS2_DAT	J9-1	PS/2 Data
HC_MDIO	49	MDIO	U2-30	Ethernet PHY Management Data I/O
HC_SD_DAT3	53	SD_DAT3	J4-1	SD 1-bit Mode: Card Detect; SPI Mode: Chip Select (Active Low)
HC_SD_CMD	44	SD_CMD	J4-2	SD 1-bit Mode: Command Line; SPI Mode: Data In
HC_SD_DAT	48	SD_DAT	J4-7	SD 1-bit Mode: Data Line; SPI Mode: Data Out
HC_SDA	50	SDA	J10-44	LCD 3-Wire Serial Interface Data

Figure 2–5 shows the Level Shift Interface schmeatic.

Figure 2–5. Level Shift Interface Schematic



Display

LCD Touch Panel Display

The board provides a 4.3" Toppoly TD043MTEA1 active matrix color display, with 800x480 pixel resolution. Table 2–7 lists LCD Touch Panel Display board reference and manufacturing information.

Table 2–7. LCD Touch Panel Display Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
Display + J10	4.3" Active Matrix Color LCD Screen (480x800 RGB) + Touch Panel	Toppoly	TD043MTEA1	www.toppoly.com
U6	12-Bit ADC for resistive touchscreen sensing	Analog Devices	AD7843	www.analog.com

The LCD panel supports the 24-bit parallel RGB data interface and provides a 3-wire interface to control the display function registers. The LCD Multimedia HSMC is also equipped with an Analog Devices AD7843 touch screen digitizer chip. The AD7843 is a 12-bit analog to digital converter (ADC) for digitizing x and y coordinates of touch points applied to the touch screen.

Timing Protocol of the LCD TDM Controller

Figure 2–6 below describes the input timing waveform information of the LCD TDM Controller implemented in the MAX II CPLD. The 8-bit wide HC_LCD_DATA signal is presumed to contain a stream of color pixel data, with each pixel represented by three successive clock-cycles of the stream. The data is presented in the order "BGR". The LCD TDM Controller uses the HC_HD pulse to determine the position of the BLUE color sample, and thus the start of each three-clock pixel-period. State transitions on HC_HD (0 →1 or 1 →0) coincide with the presentation of BLUE color on the HC_LCD_DATA input. The GREEN and RED values for that same pixel are presented on the next two clock-cycles. Figure 2–7 shows the timing information on the output side. The LCD TDM block will generate an output NCLK clock and 24-bit RGB data to the LCD panel. The NCLK signal runs at 1/3 the frequency of the incoming clock HC_NCLK.

Figure 2–6. The Timing Diagram On the Input Side of VGA TDM Controller

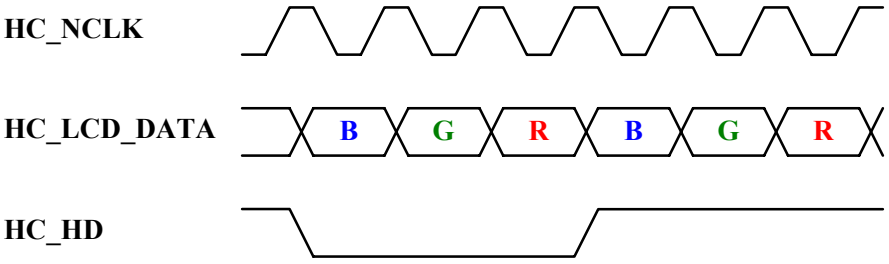
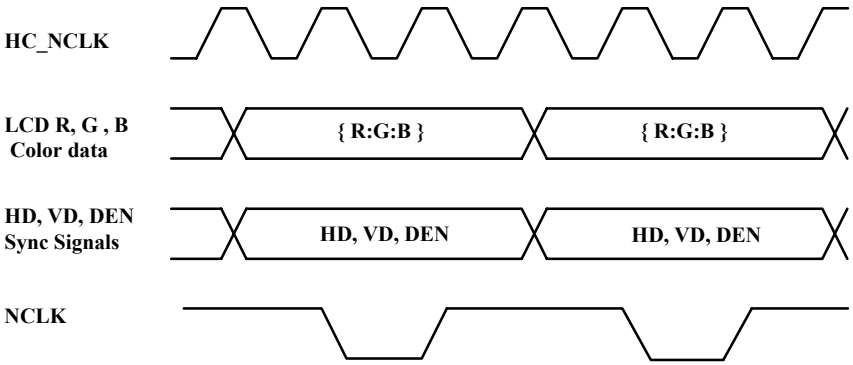


Figure 2–7. The Timing Diagram On the Output Side of VGA TDM Controller



The pin assignments are listed in Tables 2–8

Tables 2–8 shows the pinout of LCD Touch Panel with HSMC connector.

Table 2–8. LCD Touch Panel Pinout with HSMC Connector

HSMC Connector		MAX II		LCD Touch Panel		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_VD	132	D14	F6	VD	6	LCD Vertical Sync Input
HC_HD	134	C14	F5	HD	7	LCD Horizontal Sync Input

Table 2–8. LCD Touch Panel Pinout with HSMC Connector

HSMC Connector		MAX II		LCD Touch Panel		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_DEN	138	C15	E5	DEN	8	LCD RGB Data Enable
HC_NCLK	95	K13	E4	NCLK	9	LCD Clock
HC_LCD_DATA[0]	145	D17	H1	R[0]	28	LCD red data bus bit 0
			E3	G[0]	19	LCD green data bus bit 0
			D4	B[0]	10	LCD blue data bus bit 0
HC_LCD_DATA[1]	149	C17	H2	R[1]	29	LCD red data bus bit 1
			F3	G[1]	20	LCD green data bus bit 1
			C3	B[1]	11	LCD blue data bus bit 1
HC_LCD_DATA[2]	151	C16	J2	R[2]	30	LCD red data bus bit 2
			F1	G[2]	21	LCD green data bus bit 2
			C2	B[2]	12	LCD blue data bus bit 2
HC_LCD_DATA[3]	126	D13	J1	R[3]	31	LCD red data bus bit 3
			F2	G[3]	22	LCD green data bus bit 3
			D3	B[3]	13	LCD blue data bus bit 3
HC_LCD_DATA[4]	128	D15	J3	R[4]	32	LCD red data bus bit 4
			G2	G[4]	23	LCD green data bus bit 4
			D1	B[4]	14	LCD blue data bus bit 4
HC_LCD_DATA[5]	146	B15	K3	R[5]	33	LCD red data bus bit 5
			G1	G[5]	24	LCD green data bus bit 5
			D2	B[5]	15	LCD blue data bus bit 5
HC_LCD_DATA[6]	150	B14	K1	R[6]	34	LCD red data bus bit 6
			G3	G[6]	25	LCD green data bus bit 6
			E2	B[6]	16	LCD blue data bus bit 6
HC_LCD_DATA[7]	152	A15	K2	R[7]	35	LCD red data bus bit 7
			H3	G[7]	26	LCD green data bus bit 7
			E1	B[7]	17	LCD blue data bus bit 7
HC_GREST	140	C13	L2	GREST	40	LCD Global Reset, Low Active
HC_SCEN	144	B13	L1	SCEN	42	LCD 3-Wire Serial Interface Enable

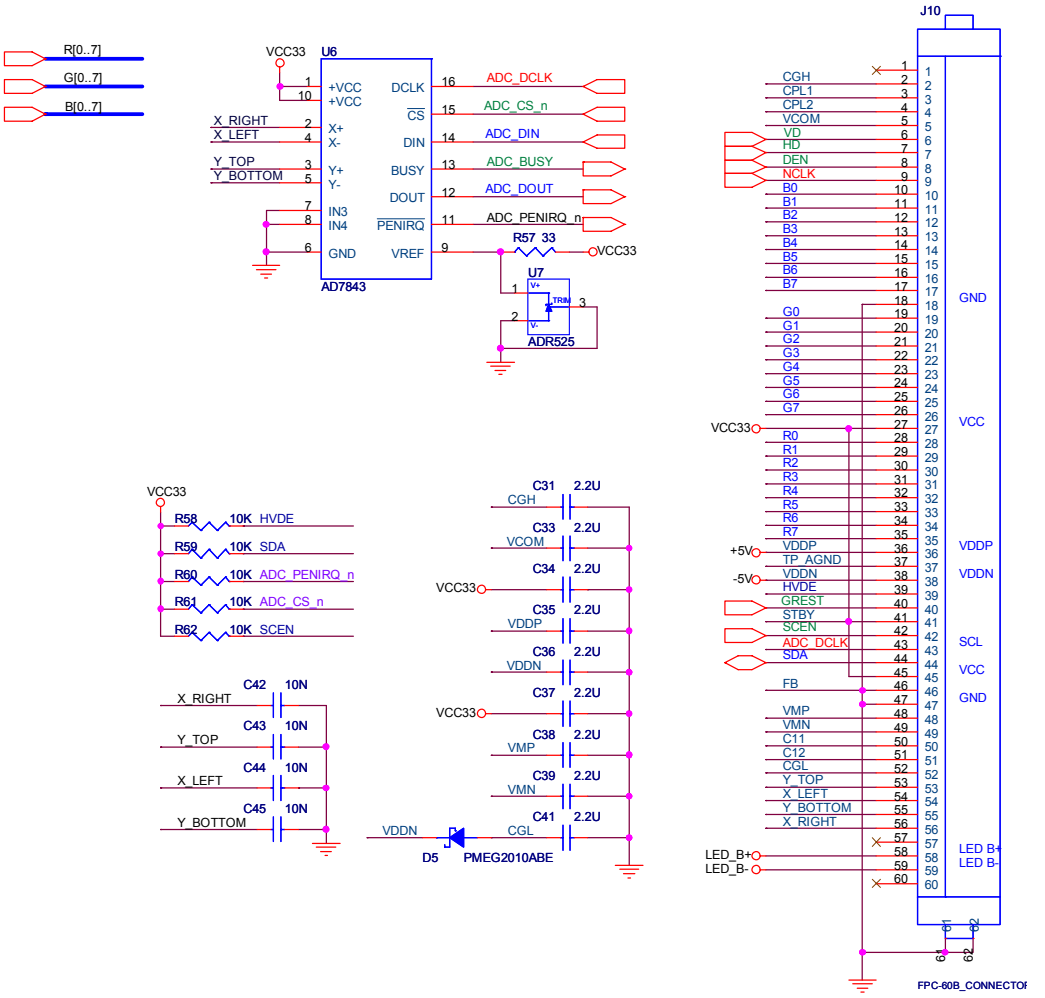
Table 2–8. LCD Touch Panel Pinout with HSMC Connector

HSMC Connector		MAX II		LCD Touch Panel		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_SDA	50	U11-5(1)	U11-10(1)	SDA	J10.44	LCD 3-Wire Serial Interface Data
HC_ADC_DCLK	157	B18	L3	ADC_DCLK	U6.16	AD7843/LCD 3-Wire Serial Interface Clock
HC_ADC_DIN	155	B16	N2	ADC_DIN	U6.14	AD7843 Serial Interface Data In
HC_ADC_CS_n	143	D18	N1	ADC_CS_n	U6.15	AD7843 Serial Interface Chip Select Input
HC_ADC_DOUT	122	E13	M1	ADC_DOUT	U6.12	AD7843 Serial Interface Data Out
HC_ADC_PENIRQ_n	156	A14	M3	ADC_PENIRQ_n	U6.11	AD7843 pen Interrupt
HC_ADC_BUSY	120	E15	M2	ADC_BUSY	U6.13	AD7843 Serial Interface Busy

Notes to Table 2–8:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U11.

Figure 2–8 shows the LCD Touch Panel schematic.

Figure 2–8. LCD Touch Panel Schematic



Interfaces/ Connectors

This section describes the following LCD Multimedia HSMC's interface/connector blocks:

- Audio Codec Interface (J1, J2, J3)
- SD Card socket (J4)
- Ethernet connector (J5)
- RS 232 connector (J8)
- UART and PS/2 connector (J9)
- Video Decoder connector (J11)
- VGA DAC connector (J12)

Audio Codec Interface

The board provides 24-bit CD-Quality audio via the Wolfson WM8731 audio CODEC (enCODer/DECoder). Table 2–9 lists Audio Codec Interface board reference and manufacturing information.

Table 2–9. Audio Codec Interface Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U1	CD quality, low power, high quality audio codec.	Wolfson Microelectronics	WM8731	www.wolfsonmicro.com

The Audio Codec Interface features:

- 24-bit sigma-delta audio CODEC
- Line-level input, line-level output, and microphone input jacks
- Sampling frequency: 8 to 96 KHz

This chip supports microphone-in (J1), audio-in (J2), and audio-out (J3) ports, with a sample rate adjustable from 8 kHz to 96 kHz. The WM8731 is controlled by a serial I2C bus interface, which is connected to pins on the HSMC connector.

Tables 2–10 shows the pinout of Audio Codec with HSMC connector.

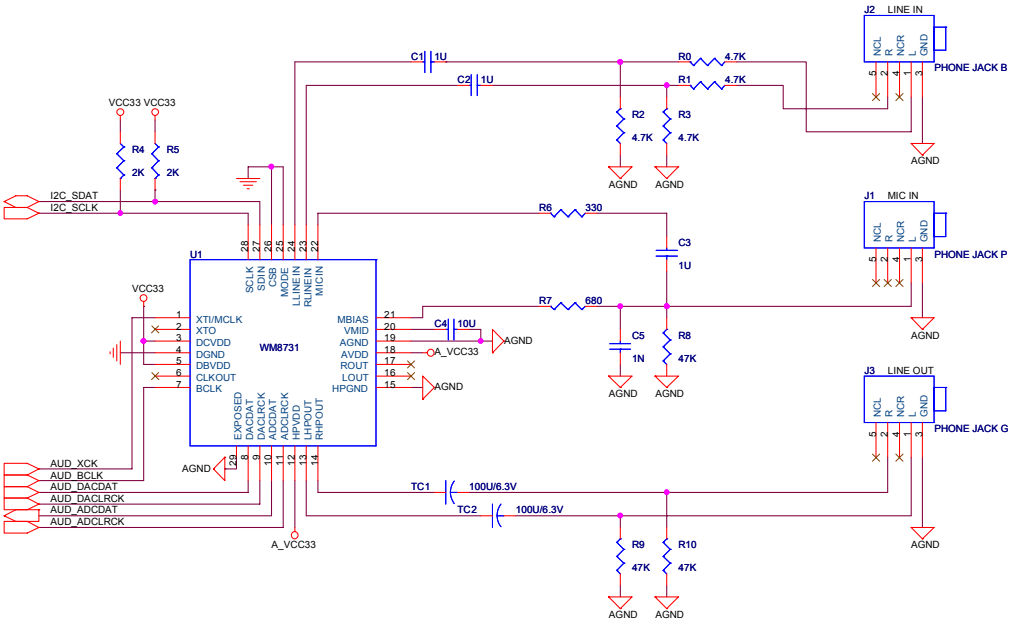
Table 2–10. Audio Codec Pinout with HSMC Connector

HSMC Connector		MAX II		Audio Codec		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_AUD_BCLK	113	G17	U13	AUD_BCLK	7	Audio CODEC Bit-Stream Clock
HC_AUD_XCK	39	T16	U14	AUD_XCK	1	Audio CODEC Chip Clock
HC_AUD_DACDAT	109	H17	V13	AUD_DACDAT	8	Audio CODEC DAC Data
HC_AUD_DACLRCK	107	H18	T13	AUD_DACLRCK	9	Audio CODEC DAC LR Clock
HC_AUD_ADCDAT	40	R15	T12	AUD_ADCDAT	10	Audio CODEC ADC Data
HC_AUD_ADCLRCK	103	H16	V12	AUD_ADCLRCK	11	Audio CODEC ADC LR Clock
HC_I2C_SDAT	33	U10-2(1)	U10-13(1)	I2C_SDAT	27	I2C Data
HC_I2C_SCLK	34	P15	U11	I2C_SCLK	28	I2C Clock

Note:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.
(2) Default, the audio chip is configured as a SLAVE mode.

Figure 2–9 shows the Audio Codec connector schematic.

Figure 2–9. Audio Codec Connector Schematic



SD Card

The board includes a SD Card socket and provides SPI mode for SD Card access. It can be accessible as memory in both SPI and and 1-bit SD mode. The SD-Card data, clock, and control signals are wired directly to the MAX II CPLD.

Tables 2–11 shows the pinout of SD Card Socket with HSMC connector.

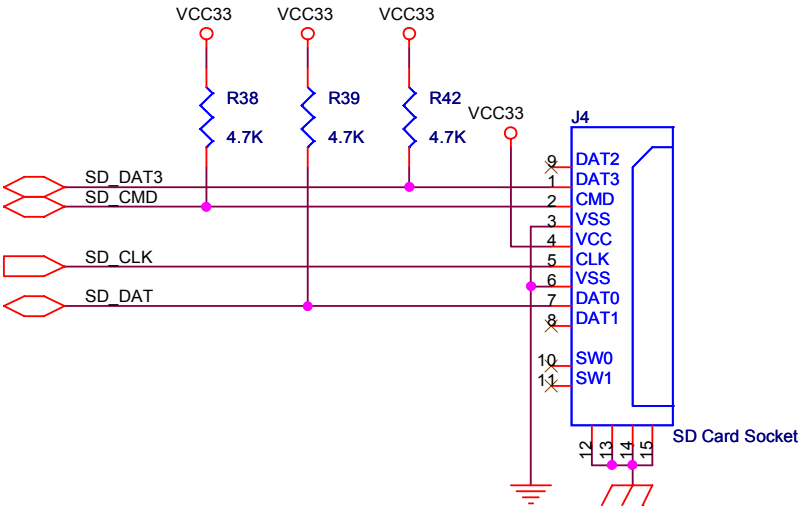
Table 2–11. SD Card Pinout with HSMC Connector

HSMC Connector		MAX II		SD Card		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_SD_DAT3	53	U11-2(1)	U11-13(1)	SD_DAT3	1	SD 1-bit Mode: Card Detect; SPI Mode: Chip Select (Active Low)
HC_SD_CMD	44	U11-3(1)	U11-12(1)	SD_CMD	2	SD 1-bit Mode: Command Line; SPI Mode: Data In
HC_SD_CLK	101	J16	P1	SD_CLK	5	Clock
HC_SD_DAT	48	U11-4(1)	U11-11(1)	SD_DAT	7	SD 1-bit Mode: Data Line; SPI Mode: Data Out

Notes:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U11.

Figure 2–10 shows the SD Card interface schematic.

Figure 2–10. SD Card Interface Schematic



Ethernet PHY

Ethernet support is provided via the National Semiconductor DP83848C Ethernet Physical Layer Transceiver chip and an RJ-45 connector (J5). Table 2–12 lists Ethernet PHY board reference and manufacturing information.

Table 2–12. Ethernet PHY Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U2	Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver	National Semiconductor	DP83848C	www.national.com

The DP83848C device has the following features:

- Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver
- Supports both 100Base-T and 10Base-T Ethernet protocols
- Supports Auto-MDIX for 10/100 Mb/s

The DP83848C is one port Fast Ethernet PHY Transceivers supporting IEEE 802.3 physical layer applications at 10 Mbps and 100 Mbps. The DP83848C provides Media Independent Interface (MII) to connect DP83848C to a MAC in the FPGA.

Tables 2–13 shows the pinout of Ethernet PHY with HSMC connector.

Table 2–13. Ethernet PHY Pinout with HSMC Connector

HSMC Connector		MAX II		Ethernet PHY		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_TX_CLK	158	A13	T2	TX_CLK	1	MII Transmit Clock
HC_TX_EN	125	F18	R3	TX_EN	2	MII Transmit Enable
HC_TXD[0]	127	F17	P4	TXD0	3	MII Transmit Data bit 0
HC_TXD[1]	131	E17	R1	TXD1	4	MII Transmit Data bit 1
HC_TXD[2]	133	E18	R2	TXD2	5	MII Transmit Data bit 2
HC_TXD[3]	137	E16	P2	TXD3	6	MII Transmit Data bit 3
HC_ETH_RESET_N	121	F16	T3	Eth_RESET_N	29	DP83848C Reset

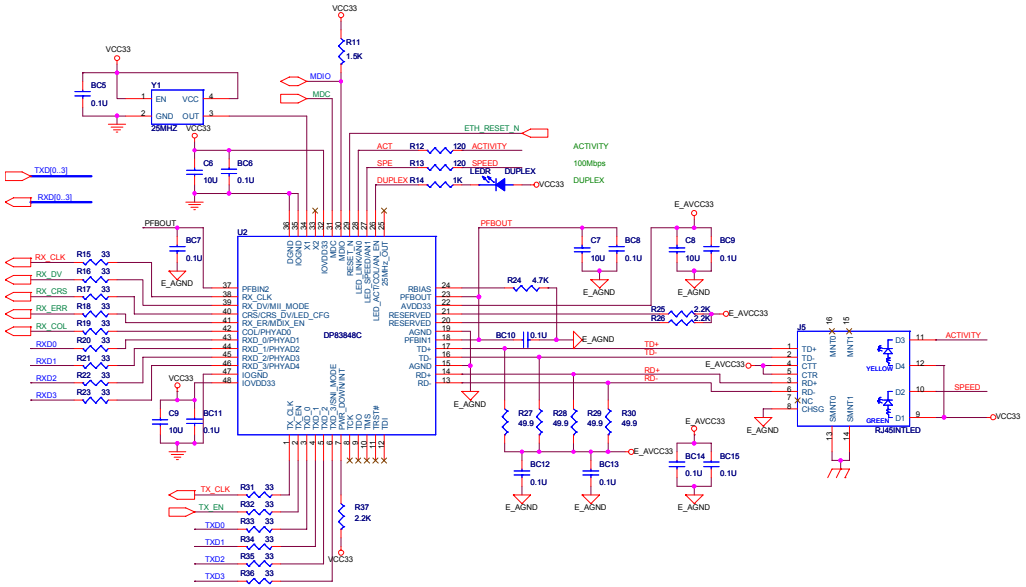
Table 2–13. Ethernet PHY Pinout with HSMC Connector

HSMC Connector		MAX II		Ethernet PHY		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_MDIO	49	U10-5(1)	U10-10(1)	MDIO	30	Management Data I/O
HC_MDC	139	D16	U1	MDC	31	Management Data Clock
HC_RX_CLK	96	H14	J5	RX_CLK	38	MII Receive Clock
HC_RX_DV	116	E14	H5	RX_DV	39	MII Receive Data valid
HC_RX_CRS	92	H15	H4	RX_CRS	40	MII Carrier Sense
HC_RX_ERR	90	G13	H6	RX_ERR	41	MII Receive Error
HC_RX_COL	114	F14	G6	RX_COL	42	MII Collision Detect
HC_RXD[0]	102	G15	G4	RXD0	43	MII Receive Data bit 0
HC_RXD[1]	104	G12	G5	RXD1	44	MII Receive Data bit 1
HC_RXD[2]	108	F13	G7	RXD2	45	MII Receive Data bit 2
HC_RXD[3]	110	F15	F4	RXD3	46	MII Receive Data bit 3

Notes:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.

Figure 2–11 shows the Ethernet PHY connector schematic.

Figure 2–11. Ethernet PHY Schematic



RS232 Serial Interface

The board uses the ADM3202 transceiver chip and a 9-pin D-SUB connector for RS-232 communications. Table 2–14 below lists RS 232 Serial Interface board reference and manufacturing information.

Table 2–14. RS232 Serial Interface Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U5	High-Speed, 2-Channel RS232/V.28 Interface Devices	Analog Devices	ADM3202	www.analog.com

Tables 2–15 shows the pinout of RS232 Interface with HSMC connector.

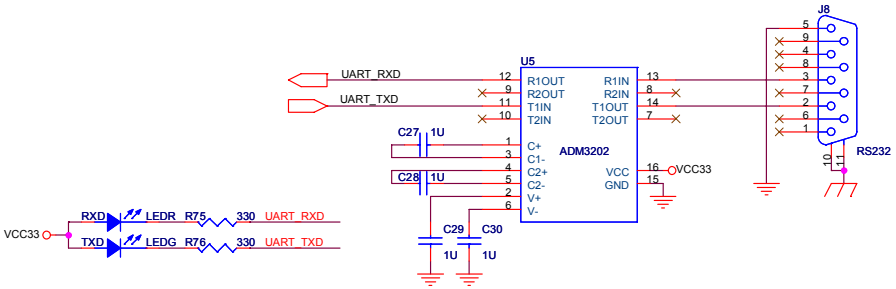
Table 2–15. RS232 Interface Pinout with HSMC Connector

HSMC Connector		MAX II		RS232 Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_UART_RXD	115	G18	K4	UART_RXD	U5-12(1)	UART Receiver
HC_UART_TXD	119	G16	J4	UART_TXD	U5-11(2)	UART Transmitter

Notes:
(1) U5.12 connects to pin 3 on the RS-232 connector (J6) via U5.13.
(2) U5.11 connects to pin 2 on the RS-232 connector (J6) via U5.14.

Figure 2–12 shows the RS232 interface schematic.

Figure 2–12. RS232 Interface Schematic



PS/2 Interface

The LCD Multimedia HSMC includes a standard PS/2 interface and a connector (J9) for a PS/2 keyboard or mouse. The PS/2 interface is a standard interface that is described extensively elsewhere. Implementation of a PS/2 interface can be done either in hardware on the MAXII or FPGA or software in a Nios processor running on the FPGA.

Tables 2–16 shows the pinout of PS/2 Interface with HSMC connector.

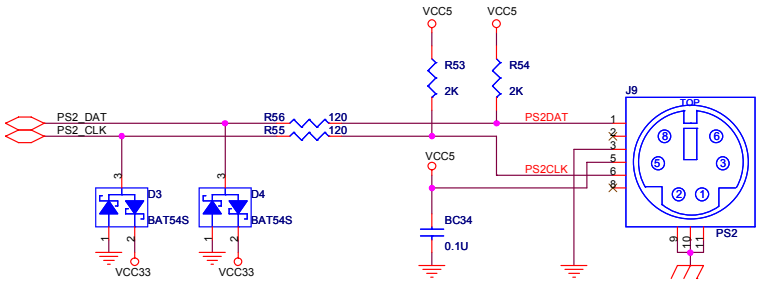
Table 2–16. PS/2 Interface Pinout with HSMC Connector

HSMC Connector		MAX II		*PS/2 Interface*		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_PS2_CLK	43	U10-3(1)	U10-12(1)	PS2_CLK	1	PS/2 Clock
HC_PS2_DAT	47	U10-4(1)	U10-11(1)	PS2_DAT	6	PS/2 Data

Notes:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.

Figure 2–13 shows the PS/2 interface schematic.

Figure 2–13. PS/2 Interface Schematic



Video Decoder Interface

The board is equipped with an Analog Devices ADV7180 Video decoder chip and RCA input jack (J11). Table 2–17 below lists Video Decoder Interface board reference and manufacturing information.

Table 2–17. Video Decoder Interface

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U8	10-Bit, 4× Oversampling SDTV Video Decoder	Analog Devices	ADV7180	www.analog.com

The Video Decoder features:

- Multi-format SDTV Video Decoder
- Supports worldwide NTSC/PAL/SECAM color demodulation
- One 10-bit ADC, 4X over-sampling for CVBS
- Supports Composite Video (CVBS) RCA jack input
- Supports digital output formats: 8-bit ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD

The ADV7180 is an integrated video decoder that automatically detects and converts a standard analog baseband television signal (NTSC, PAL, and SECAM) into 4:2:2 component video data compatible with 8-bit CCIR601/CCIR656. The ADV7180 is compatible with a broad range of video devices, including DVD players, tape-based sources, broadcast sources, and security/surveillance cameras.

The registers in the Video decoder can be programmed by a serial I2C bus, which is connected to the HSMC connector as indicated in schematic.

Tables 2–18 shows the pinout of Video Decoder with HSMC connector.

Table 2–18. Video Decoder Pinout with HSMC Connector

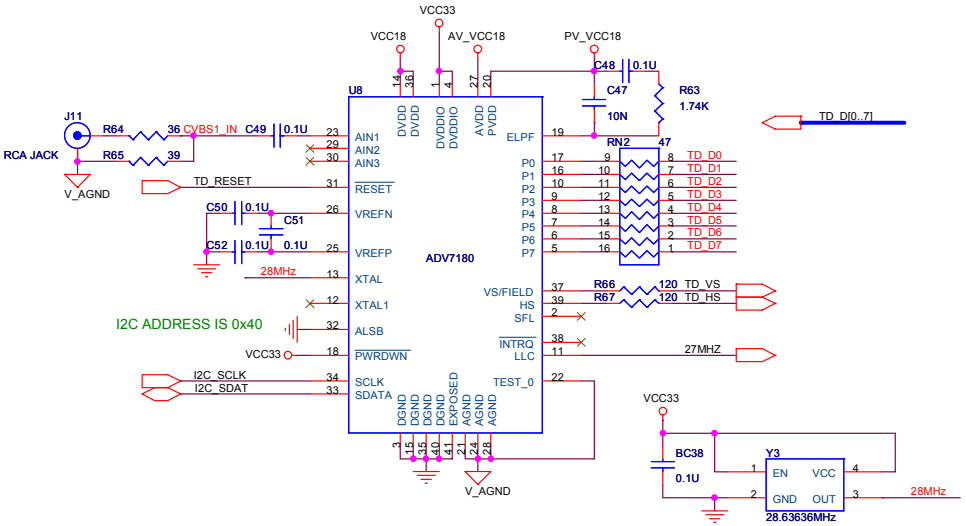
HSMC Connector		MAX II		Video Decoder		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_TD_D[7]	78	K14	T10	TD_D7	5	Video Decoder Data[7]
HC_TD_D[6]	74	K15	V10	TD_D6	6	Video Decoder Data[6]
HC_TD_D[5]	72	L13	U10	TD_D5	7	Video Decoder Data[5]
HC_TD_D[4]	68	M12	U9	TD_D4	8	Video Decoder Data[4]
HC_TD_D[3]	66	L15	V9	TD_D3	9	Video Decoder Data[3]
HC_TD_D[2]	62	L14	T9	TD_D2	10	Video Decoder Data[2]
HC_TD_D[1]	60	M14	T8	TD_D1	16	Video Decoder Data[1]
HC_TD_D[0]	56	M15	V8	TD_D0	17	Video Decoder Data[0]
HC_TD_27MHZ	98	G14	U8	TD_27MHZ	11	Video Decoder Clock Input
HC_TD_RESET	80	J14	U12	TD_RESET	31	Video Decoder Reset
HC_I2C_SDAT	33	U10-2(1)	U10-13(1)	I2C_DATA	33	I2C Data
HC_I2C_SCLK	34	P15	U11	I2C_SCLK	34	I2C Clock
HC_TD_VS	84	J15	V11	TD_VS	37	Video Decoder V_SYNC

Table 2–18. Video Decoder Pinout with HSMC Connector						
HSMC Connector		MAX II		Video Decoder		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_TD_HS	86	H13	T11	TD_HS	39	Video Decoder H_SYNC

Notes:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.

Figure 2–14 shows the Video Decoder interface schematic.

Figure 2–14. Video Decoder Interface Schematic



NTSC PAL Video Decoder Circuit

Uses the ADV7180 Multi-format SDTV Video Decoder

- Supports worldwide NTSC/PAL/SECAM color demodulation
- One 10-bit ADC, 4X over-sampling for CVBS
- Supports Composite Video (CVBS) RCA jack input
- Supports digital output formats: 8-bit ITU-R BT.656 YCrCb 4:2:2

- output + HS, VS, and FIELD
- Applications: DVD recorders, LCD TV, Set-top boxes, Digital TV
- Portable video devices

VGA DAC Interface

The board includes an Analog Devices ADV7123 VGA DAC and 16-pin D-SUB connector for VGA output. Table 2–19 below lists VGA DAC Interface board reference and manufacturing information.

Table 2–19. VGA Output DAC

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U9	240 MHz Triple 10-Bit High Speed Video DAC	Analog Devices	ADV7123	www.analog.com

The VGA DAC interface features:

- 240-MHz triple 10-bit high-speed video DAC
- 15-pin high-density D-sub connector

The VGA synchronization signals are provided directly from the Cyclone III FPGA, and the Analog Devices ADV7123 triple 10-bit high-speed video DAC is used to produce the analog data signals (red, green, and blue).

Figure 2–15 illustrates the basic timing requirements for each row (horizontal) that is displayed on a VGA monitor. An active-low pulse of specific duration (time) as shown in the figure is applied to the horizontal synchronization (hsync) input of the monitor, which signifies the end of one row of data and the start of the next. The data (RGB) inputs on the monitor must be off (driven to 0 V) for a time period called the back porch (b) after the hsync pulse occurs, which is followed by the display interval (c). During the data display interval, the RGB data drives each pixel in turn across the row being displayed. Finally, there is a time period called the front porch (d) where the RGB signals must again be off before the next hsync pulse can occur. The timing of the vertical synchronization (vsync) is the same as shown in Figure 2–15, except that a vsync pulse signifies the end of one frame and the start of the next, and the data refers to the set of rows in the frame (horizontal timing). Table 2–20 and Table 2–21 show, for different resolutions, the durations of time periods a, b, c, and d for both horizontal and vertical timing.

On the LCD Multimedia HSMC users still need to multiplex the VGA synchronization and RGB data to fit the VGA TDM block input timing as mentioned in Figure 2–6 and Figure 2–7. The timing protocol of the VGA TDM controller is similar to the LCD TDM controller. The input color data bus HC_VGA_DATA changes from 8-bit to 10-bit, and the VGA TDM controller uses the HC_VGA_HS to determine the position of the BLUE color sample.

Figure 2–15. V.G.A. Horizontal Timing Specification

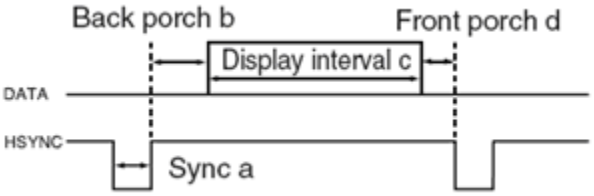


Table 2–20. VGA Horizontal Timing Specification

Configuration	Resolution(HxV)	a(us)	b(us)	c(us)	d(us)	Pixel clock(Mhz)
VGA(60Hz)	640x480	3.8	1.9	25.4	0.6	25 (640/c)
VGA(85Hz)	640x480	1.6	2.2	17.8	1.6	36 (640/c)
SVGA(60Hz)	800x600	3.2	2.2	20	1	40 (800/c)
SVGA(75Hz)	800x600	1.6	3.2	16.2	0.3	49 (800/c)
SVGA(85Hz)	800x600	1.1	2.7	14.2	0.6	56 (800/c)
XGA(60Hz)	1024x768	2.1	2.5	15.8	0.4	65 (1024/c)
XGA(70Hz)	1024x768	1.8	1.9	13.7	0.3	75 (1024/c)
XGA(85Hz)	1024x768	1.0	2.2	10.8	0.5	95 (1024/c)
1280x1024(60Hz)	1280x1024	1.0	2.3	11.9	0.4	108 (1280/c)

Table 2–21. VGA Vertical Timing Specification

Configuration	Resolution (HxV)	a(lines)	b(lines)	c(lines)	d(lines)
VGA(60Hz)	640x480	2	33	480	10
VGA(85Hz)	640x480	3	25	480	1
SVGA(60Hz)	800x600	4	23	600	1

Table 2–21. VGA Vertical Timing Specification

Configuration	Resolution (HxV)	a(lines)	b(lines)	c(lines)	d(lines)
SVGA(75Hz)	800x600	3	21	600	1
SVGA(85Hz)	800x600	3	27	600	1
XGA(60Hz)	1024x768	6	29	768	3
XGA(70Hz)	1024x768	6	29	768	3
XGA(85Hz)	1024x768	3	36	768	1
1280x1024(60Hz)	1280x1024	3	38	1024	1

Tables 2–22 shows the pinout of VGA/DAC Interface with HSMC connector.

Table 2–22. VGA/DAC Interface Pinout with HSMC Connector

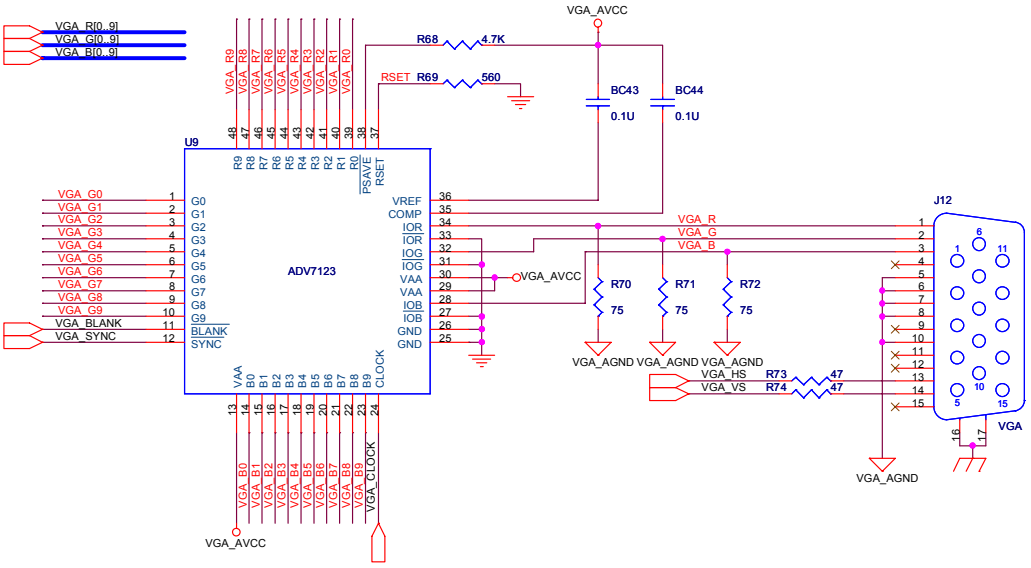
HSMC Connector		MAX II		VGA/DAC Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_VGA_DATA[0]	65	N16	U7	VGA_R0	39	VGA red data bus bit 0
			V4	VGA_G0	1	VGA green data bus bit 0
			R7	VGA_B0	14	VGA blue data bus bit 0
HC_VGA_DATA[1]	67	M16	V7	VGA_R1	40	VGA red data bus bit 1
			U4	VGA_G1	2	VGA green data bus bit 1
			P6	VGA_B1	15	VGA blue data bus bit 1
HC_VGA_DATA[2]	71	M18	T7	VGA_R2	41	VGA red data bus bit 2
			U3	VGA_G2	3	VGA green data bus bit 2
			R6	VGA_B2	16	VGA blue data bus bit 2
HC_VGA_DATA[3]	73	M17	T6	VGA_R3	42	VGA red data bus bit 3
			V2	VGA_G3	4	VGA green data bus bit 3
			R5	VGA_B3	17	VGA blue data bus bit 3
HC_VGA_DATA[4]	77	L17	V6	VGA_R4	43	VGA red data bus bit 4
			P8	VGA_G4	5	VGA green data bus bit 4
			N4	VGA_B4	18	VGA blue data bus bit 4
HC_VGA_DATA[5]	79	L18	U6	VGA_R5	44	VGA red data bus bit 5
			R9	VGA_G5	6	VGA green data bus bit 5
			N5	VGA_B5	19	VGA blue data bus bit 5

Table 2–22. VGA/DAC Interface Pinout with HSMC Connector

HSMC Connector		MAX II		VGA/DAC Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_VGA_DATA[6]	83	L16	U5	VGA_R6	45	VGA red data bus bit 6
			P9	VGA_G6	7	VGA green data bus bit 6
			M5	VGA_B6	20	VGA blue data bus bit 6
HC_VGA_DATA[7]	85	K16	V5	VGA_R7	46	VGA red data bus bit 7
			P10	VGA_G7	8	VGA green data bus bit 7
			M4	VGA_B7	21	VGA blue data bus bit 7
HC_VGA_DATA[8]	89	K18	T5	VGA_R8	47	VGA red data bus bit 8
			R10	VGA_G8	9	VGA green data bus bit 8
			M6	VGA_B8	22	VGA blue data bus bit 8
HC_VGA_DATA[9]	91	J18	T4	VGA_R9	48	VGA red data bus bit 9
			P11	VGA_G9	10	VGA green data bus bit 9
			L6	VGA_B9	23	VGA blue data bus bit 9
HC_VGA_BLANK	59	N17	R8	VGA_BLANK	11	VGA BLANK
HC_VGA_SYNC	61	N18	P7	VGA_SYNC	12	VGA SYNC
HC_VGA_CLOCK	97	J13	L4	VGA_CLOCK	24	VGA TDM Clock

Figure 2–16 shows the VGA/DAC interface schematic.

Figure 2–16. VGA/DAC Interface Schematic



Clocking Circuitry

The board has a number of dedicated clock oscillators that are used for system timing or timing of specific peripheral chips. A list of these oscillators is shown in Table 2–23 below.

Table 2–23. Oscillators

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
Y1	25MHz, 25ppm, CL=15pF, 3.3V, Size:5*7*1.4 mm	Mercury Electronics	FH3SWO-AT-25.000	www.mecxtal.com
Y2	100MHz, 25ppm, CL=15pF, 3.3V, Size:5*7*1.4 mm	Mercury Electronics	FH3SWO-AT-100.000	www.mecxtal.com
Y3	28MHz, 25ppm, CL=15pF, 3.3V, Size:5*7*1.4 mm	Mercury Electronics	FH3SWO-AT-27.000	www.mecxtal.com

Power Supply

Power Supplies

The power supply block distributes clean power from the 12 V and 3.3 V input supply (from HSMC connector) to the LCD Multimedia HSMC through on-board regulators. To provide various voltage options, the board uses several Linear Technologies' regulators. Switching regulators are used for digital circuits and linear regulators are used for analog circuits.

Table 2–24 below lists Power Supplies board reference and manufacturing information.

Table 2–24. Power Supplies Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
REG1	DC/DC Converter +/- 5V for LCD Display	Linear Technology	LT3461ES6#TRPBF	www.linear.com
REG2	DC/DC Converter for +/- Voltages for LCD Display Backlight	Linear Technology	LT3461ES6#TRPBF	www.linear.com
REG3	Linear regulator for 5V output	Linear Technology	LT1117CTS-5#PBF	www.linear.com
REG4	Linear regulator for 2.5V output	Linear Technology	LT1963AES8#PBF	www.linear.com
REG5	Linear regulator for 1.8V output	Linear Technology	LT1963AES8#PBF	www.linear.com

Board regulators are used to generate the voltages listed in Tables 2–25

Table 2–25. Board Regulators

Output Voltage (V)	Variance (+/-mV)	MAX Current (A)	Regulator Board Reference	Linear Technologies Part #	Where Used
5V	50 mV	115mA	REG1	LT3461ES6#TRPBF	LCD Supply
26.4V	100mV	-	REG2	LT3461ES6#TRPBF	LED Backlight
5V	50mV	800mA	REG3	LT1117CTS-5#PBF	PS2 Interface Supply
2.5V	27mV	1.5A	REG4	LT1963AES8#PBF	CPLD Bank Supply, Level Shifter Supply
1.8V	27mV	1.5A	REG5	LT1963AES8#PBF	Video Decoder Supply

EEPROM

I2C Serial EEPROM

There is a 2K-bits I2C Serial EEPROM on the LCD Multimedia HSMC that contains information used by applications for this board. Table 2–26 below lists I2C Serial EEPROM board reference and manufacturing information.

Table 2–26. I2C Serial EEPROM Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U3	2K-bits I2C Serial EEPROM	Microchip	24LC02B	www.microchip.com

Table 2–27 contains the data format written in the first 16 bytes of this EEPROM.

Table 2–27. EEPROM Data Format

Byte #s	Bit #s	Description	Value for LCD Multimedia HSMC
0	0-7	Number of bytes written (including Byte 0)	0x10
1(1)	0-3	Minor revision number	0x0
	4-7	Major revision number	0x1
2-7	0-7	Board Serial Number (If bytes 2-4 is “00 07 ED” then this is a MAC address.)	Altera MAC Addresses are in the format “00 07 ED 08 xx xx”. The "08" is the group for the LCD Multimedia HSMC. The last two bytes are sequential and incremented for each board.
8-15	0-7	8 bytes of board specific calibration data.	Calibration Data for TouchScreen is currently in the form of Upper Right X (3946 = 0x0f6a), Upper Right Y (3849 = 0x0f09), Lower Left X (132 = 0x0084), Lower Left Y (148 = 0x0094)

Notes:
(1) Version Number in the form of <Major>.<Minor>.

To provide better accuracy for the touch-screen portion of the LCD module, static calibration data has been programmed in bytes 8-15 of the EEPROM. This data is shown in Table 2–28.

Table 2–28. Byte values for touch screen calibration data

Byte	8	9	10	11	12	13	14	15
Value	0f	6a	0f	09	00	84	00	94
Coordinate	x=799		y=0		x=0		y=479	
Position	Upper Right				Lower Left			

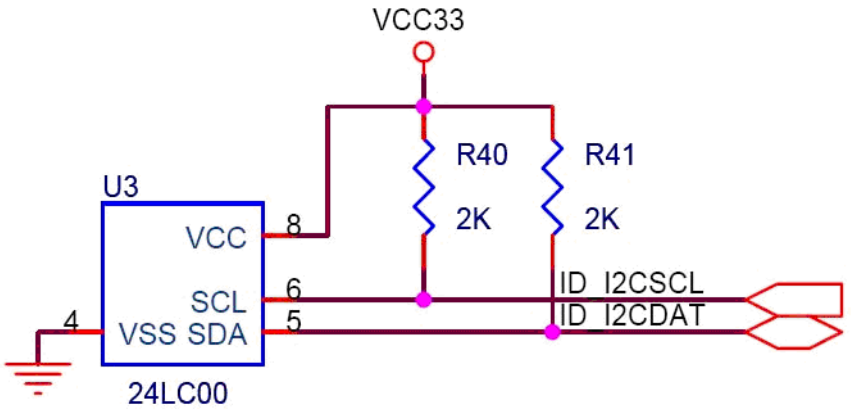
Table 2–29 shows the pinout of I2C Serial EEPROM with HSMC connector.

Table 2–29. I2C Serial EEPROM Pinout with HSMC Connector

I2C Serial EEPROM		MAX II		I2C Serial EEPROM		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_ID_I2CSCL	41	T17	N3	ID_I2CSCL	6	EEPROM I2C Clock
HC_ID_I2CDAT	42	P18	P3	ID_I2CDAT	5	EEPROM I2C Data

Figure 2–17 shows the I2C Serial EEPROM schematic.

Figure 2–17. I2C Serial EEPROM Schematic



Expansion Interface

HSMC Interface

The LCD Multimedia HSMC connects to Altera FPGA Starter and Development Boards via a single High Speed Mezzanine Card (HSMC) connector (J6).

Table 2–30 below lists HSMC A connector board reference and manufacturing information.

Table 2–30. HSMC A Connector Manufacturing Information

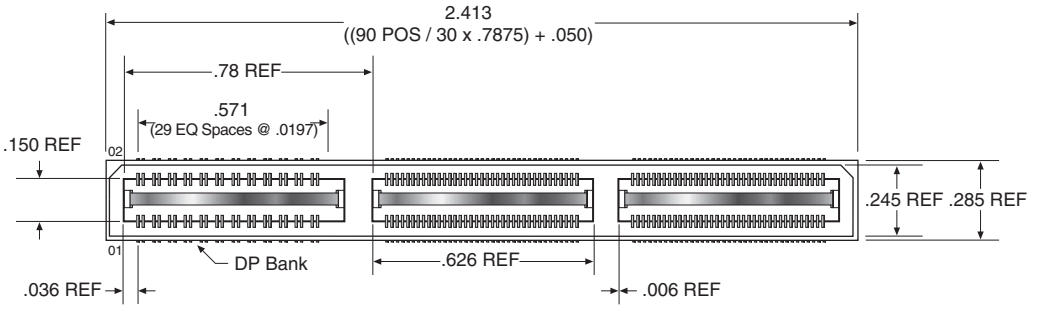
Board Reference	Description	Manufacturer	Manufacturer Part Number
J6	High Speed Mezzanine Card Connector	Samtec	ASP-122952-01

The HSMC connector is a modified version of standard high-speed Samtec connectors. To provide better integrity between host boards and HSMC boards when using high-speed transceivers, the standard high-speed Samtec connector is modified by removing every third pin in bank 1.

CMOS utilization of the HSMC pins is assumed and no options for supporting other differential signaling are provided with the board. The eight clock-data-recovery high-speed transceiver channels are not connected on this HSMC.

The HSMC connector layout is shown in Figures 2–18 below.

Figure 2–18. Samtec Header Connector



HSMC connector pinout information is shown throughout this document for each individual interface and in the appendices for connecting to various FPGA starter and development boards.

Statement of China-RoHS Compliance

Table 2–31 lists hazardous substances included with the kit.

Table 2–31. Table of Hazardous Substances' Name and Concentration, Notes (1),(2)

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone III FPGA starter board	X*	0	0	0	0	0
12 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–31:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

Appendix A. Pin Connections HSMC →FPGA for the Cyclone III Starter Board

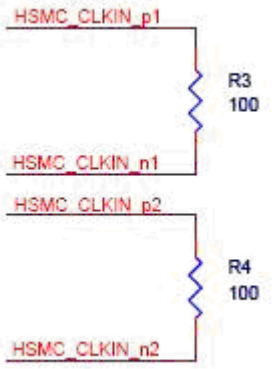
Introduction

The section describes the HSMC pin connections for Cyclone III Starter Board. See Tables A–2

Special caution when building applications with the LCD Multimedia HSMC and the Cyclone III FPGA Starter Board:

CAUTION

The LCD Multimedia HSMC uses the differential pair HSMC_CLKIN pins as single-ended I/O. On the Cyclone III Starter Board, the n and p signals for these pins are terminated with 100 Ohm resistors (R3 and R4).



These signals correspond to single-ended I/O on the LCD Multimedia HSMC. R3 connects HC_RX_CLK and HC_TD_27MHZ and R4 connects HC_ADC_PENIRQ_n and HC_TX_CLK. To avoid unwanted noise on signals, users are advised to turn off the peripherals as shown in the Table A–1 below.

☞ The Cyclone III FPGA Starter Board schematic can be found at:<*installation directory*>/board_design_files/schematic/cycloneIII_3c25_start.

Table A–1. Settings to avoid unwanted noise across signals		
When using this function	**Disable this chip**	**Required Setting**
Video Decoder	Ethernet PHY (U2)	Set **HC_ETH_RESET_N** to logic 0
Touch Panel	Ethernet PHY (U2)	Set **HC_ETH_RESET_N** to logic 0
Ethernet PHY	Video Decoder (U8)	Set **HC_TD_RESET** to logic 0 **Avoid** using touch-panel.

Table A–2. HSMC→FPGA Pinout				
Signal Name	**HSMC Pin**	**FPGA Pin**	**Direction**	**Type**
HSMC_SDA	33	E1	Bidirectional	2.5 V
HSMC_SCL	34	F3	Bidirectional	2.5 V
HSMC_TCK	35	J1		
HSMC_TMS	36	J2		
HSMC_TDI	37	J6		
HSMC_TDO	38	J5		
HSMC_CLKOUT0	39	A1	Output	2.5 V
HSMC_CLKIN0	40	A9	Input	2.5 V
HSMC_CLKOUT_p1	95	D14	Output	2.5 V
HSMC_CLKIN_p1	96	F17	Input	2.5 V
HSMC_CLKOUT_n1	97	C14	Output	2.5 V
HSMC_CLKIN_n1	98	F18	Input	2.5 V
HSMC_CLKOUT_p2	155	U18	Output	2.5 V
HSMC_CLKIN_p2	156	N17	Input	2.5 V
HSMC_CLKOUT_n2	157	V18	Output	2.5 V
HSMC_CLKIN_n2	158	N18	Input	2.5 V
HSMC_D0	41	H6	Bidirectional	2.5 V
HSMC_D1	42	D3	Bidirectional	2.5 V
HSMC_D2	43	M5	Bidirectional	2.5 V
HSMC_D3	44	L6	Bidirectional	2.5 V
HSMC_D4	47	T1	Bidirectional	2.5 V

Table A–2. HSMC→FPGA Pinout

Signal Name	HSMC Pin	FPGA Pin	Direction	Type
HSMC_D5	48	M3	Bidirectional	2.5 V
HSMC_D6	49	N7	Bidirectional	2.5 V
HSMC_D7	50	T2	Bidirectional	2.5 V
HSMC_D8	53	N8	Bidirectional	2.5 V
HSMC_D9	54	H15	Bidirectional	2.5 V
HSMC_D10	55	J13	Bidirectional	2.5 V
HSMC_D11	56	H16	Bidirectional	2.5 V
HSMC_D12	59	N10	Bidirectional	2.5 V
HSMC_D13	60	N16	Bidirectional	2.5 V
HSMC_D14	61	N11	Bidirectional	2.5 V
HSMC_D15	62	N15	Bidirectional	2.5 V
HSMC_D16	65	K17	Bidirectional	2.5 V
HSMC_D17	66	R16	Bidirectional	2.5 V
HSMC_D18	67	P11	Bidirectional	2.5 V
HSMC_D19	68	T16	Bidirectional	2.5 V
HSMC_TX_p4	71	B2	Bidirectional	2.5 V
HSMC_RX_p4	72	C2	Bidirectional	2.5 V
HSMC_TX_n4	73	B1	Bidirectional	2.5 V
HSMC_RX_n4	74	C1	Bidirectional	2.5 V
HSMC_TX_p5	77	G2	Bidirectional	2.5 V
HSMC_RX_p5	78	H2	Bidirectional	2.5 V
HSMC_TX_n5	79	G1	Bidirectional	2.5 V
HSMC_RX_n5	80	H1	Bidirectional	2.5 V
HSMC_TX_p6	83	K2	Bidirectional	2.5 V
HSMC_RX_p6	84	K5	Bidirectional	2.5 V
HSMC_TX_n6	85	K1	Bidirectional	2.5 V
HSMC_RX_n6	86	L5	Bidirectional	2.5 V
HSMC_TX_p7	89	L2	Bidirectional	2.5 V
HSMC_RX_p7	90	L4	Bidirectional	2.5 V
HSMC_TX_n7	91	L1	Bidirectional	2.5 V
HSMC_RX_n7	92	L3	Bidirectional	2.5 V
HSMC_TX_p8	101	M2	Bidirectional	2.5 V
HSMC_RX_p8	102	P2	Bidirectional	2.5 V

Table A–2. HSMC→FPGA Pinout				
Signal Name	**HSMC Pin**	**FPGA Pin**	**Direction**	**Type**
HSMC_TX_n8	103	M1	Bidirectional	2.5 V
HSMC_RX_n8	104	P1	Bidirectional	2.5 V
HSMC_TX_p9	107	R2	Bidirectional	2.5 V
HSMC_RX_p9	108	T3	Bidirectional	2.5 V
HSMC_TX_n9	109	R1	Bidirectional	2.5 V
HSMC_RX_n9	110	R3	Bidirectional	2.5 V
HSMC_TX_p10	113	E17	Bidirectional	2.5 V
HSMC_RX_p10	114	G17	Bidirectional	2.5 V
HSMC_TX_n10	115	E18	Bidirectional	2.5 V
HSMC_RX_n10	116	G18	Bidirectional	2.5 V
HSMC_TX_p11	119	H17	Bidirectional	2.5 V
HSMC_RX_p11	120	K18	Bidirectional	2.5 V
HSMC_TX_n11	121	H18	Bidirectional	2.5 V
HSMC_RX_n11	122	L18	Bidirectional	2.5 V
HSMC_TX_p12	125	L17	Bidirectional	2.5 V
HSMC_RX_p12	126	L16	Bidirectional	2.5 V
HSMC_TX_n12	127	M18	Bidirectional	2.5 V
HSMC_RX_n12	128	M17	Bidirectional	2.5 V
HSMC_TX_p13	131	L14	Bidirectional	2.5 V
HSMC_RX_p13	132	L13	Bidirectional	2.5 V
HSMC_TX_n13	133	L15	Bidirectional	2.5 V
HSMC_RX_n13	134	M14	Bidirectional	2.5 V
HSMC_TX_p14	137	P17	Bidirectional	2.5 V
HSMC_RX_p14	138	R17	Bidirectional	2.5 V
HSMC_TX_n14	139	P18	Bidirectional	2.5 V
HSMC_RX_n14	140	R18	Bidirectional	2.5 V
HSMC_TX_p15	143	R5	Bidirectional	2.5 V
HSMC_RX_p15	144	M6	Bidirectional	2.5 V
HSMC_TX_n15	145	R4	Bidirectional	2.5 V
HSMC_RX_n15	146	N6	Bidirectional	2.5 V
HSMC_TX_p16	149	T17	Bidirectional	2.5 V
HSMC_RX_p16	150	M13	Bidirectional	2.5 V

Table A–2. HSMC→FPGA Pinout

Signal Name	HSMC Pin	FPGA Pin	Direction	Type
HSMC_TX_n16	151	T18	Bidirectional	2.5 V
HSMC_RX_n16	152	N13	Bidirectional	2.5 V

Additional Information

Revision History

The table below displays the revision history for the chapters of the kit.

Chapter	Date	Version	Changes Made
All	August 2008	1.0.1	• Replaced LCD Multimedia Daughtercard with LCD Multimedia HSMC. • Modified Warning in Appendix-A. • Modified Document Part No.
All	November 2007	1.0.0	• First publication.

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Information Type	Contact *Note (1)*
Technical support	www.altera.com/mysupport/
Technical training	www.altera.com/training/
Technical training services	custrain@altera.com
Product literature	www.altera.com/literature
Product literature services	literature@altera.com
FTP site	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.

Visual Cue	Meaning
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
WARNING	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.